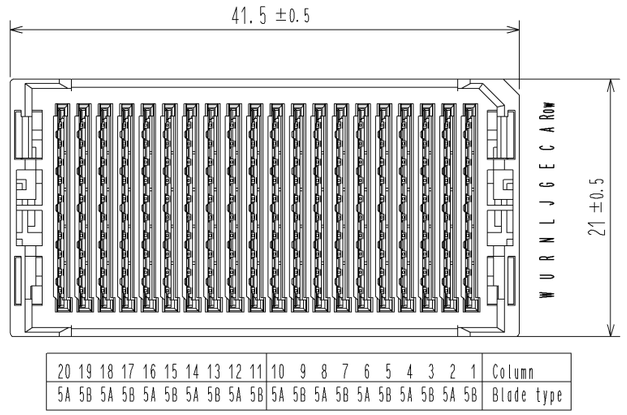
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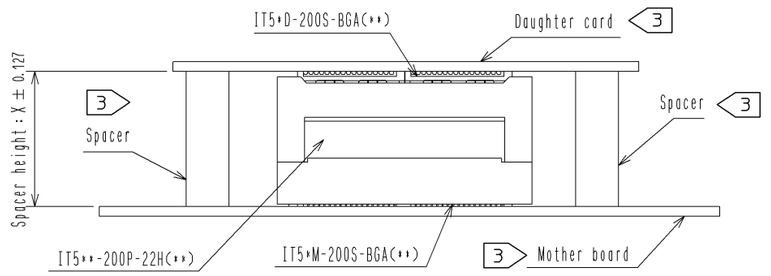
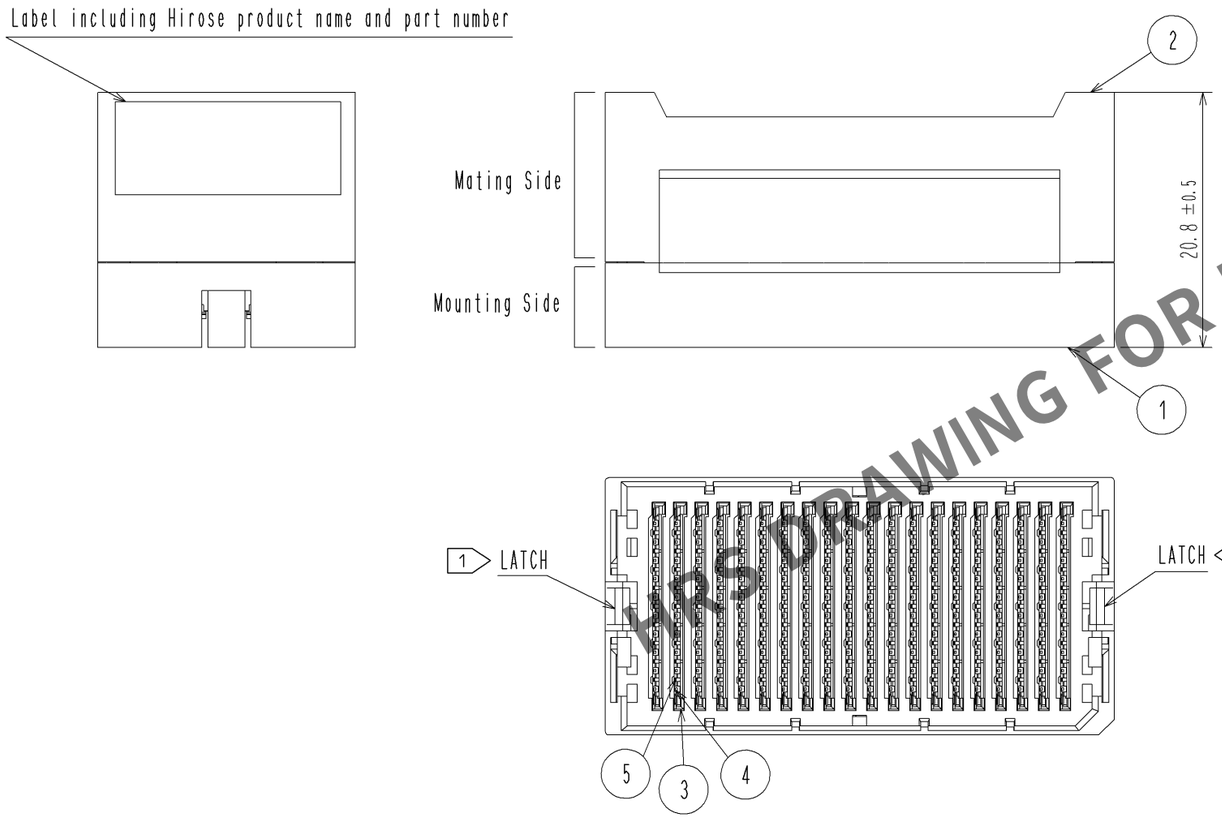
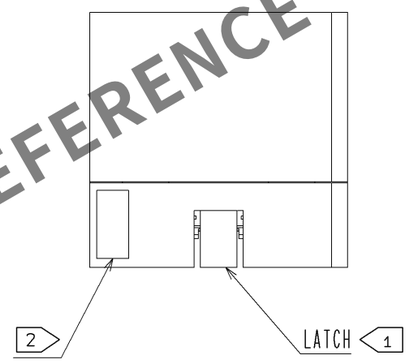


Fig.1 (FREE)





HRS DRAWING FOR REFERENCE

Receptacle Detachable(mating) side	Interposer	Receptacle Mounting side	Spacer height(X)
IT5D-200S-BGA(**)	IT5**-200P-22H(**)	IT5M-200S-BGA(**)	22
		IT5HM-200S-BGA(**)	23
IT5HD-200S-BGA(**)		IT5M-200S-BGA(**)	
		IT5HM-200S-BGA(**)	24

Table1 Spacer height

NOTE. 1 Mounting side is mated with the receptacle:IT5*M-200S-BGA(**) and fixed with the latch.
2 Lot No. shall be marked on the indicated position.
3 The indicated mother board and daughter card shall be fastened to the additional reinforcements to prevent the stress on IT5**-200S-BGA(**) solder joints.
4. Please refer to HIROSE document: ETAD-F0584 'IT5 design guideline'.
5. This product consists of 200 signal lines.
6. 40pcs of this products are packed in a soft tray.
7. Standard package of 80pcs are packaged in a carton box.
8 Please contact Hirose regarding pin assignment for single-ended signal transmission at the pairs used for differencial signal transmission.

NO.	MATERIAL	FINISH , REMARKS
3	LCP	BLACK, UL94V-0
2	PBT	GRAY, UL94V-0
1	PBT	BLACK, UL94V-0

NO.	MATERIAL	FINISH , REMARKS
5	Copper Alloy	Contact area:Nickel(1.5μm)+Gold(0.76μm)
		Other area :Nickel(1.5μm)
4	Copper Alloy	Contact area:Nickel(1.5μm)+Gold(0.76μm)
		Other area :Nickel(1.5μm)

UNITS mm	SCALE 2 : 1	COUNT	DESCRIPTION OF REVISIONS	DESIGNED	CHECKED	DATE

HIROSE ELECTRIC CO., LTD.

APPROVED	MK. EZAKI	14. 07. 08
CHECED	MK. EZAKI	14. 07. 08
DESIGNED	TF. SUGAWARA	14. 07. 07
DRAWN	TF. SUGAWARA	14. 07. 07

DRAWING NO.	EDC3-341399-01
PART NO.	IT5-200P-22H(03)
CODE NO.	CL636-1049-4-03

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FOR REFERENCE
HRS DRAWING

Wafer type	Wafer #	Column 40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Row
IT5 wafer A (100 ohm)	20	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	19	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	A
IT5 wafer A (100 ohm)	18	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	17	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	B
IT5 wafer A (100 ohm)	16	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	15	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	C
IT5 wafer A (100 ohm)	14	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	13	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	D
IT5 wafer A (100 ohm)	12	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	11	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	E
IT5 wafer A (100 ohm)	10	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	9	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	F
IT5 wafer A (100 ohm)	8	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	7	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G
IT5 wafer A (100 ohm)	6	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	5	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	H
IT5 wafer A (100 ohm)	4	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	3	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	J
IT5 wafer A (100 ohm)	2	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	G	P	X
IT5 wafer B (100 ohm)	1	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	G	N	K

IT5*M-200S-BGA(**) Pin assignment footprint for mounting side

Wafer type	Wafer #	Column 40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Row
IT5 wafer A (100 ohm)	20	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	Y
IT5 wafer B (100 ohm)	19	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	G	X	G	P	W
IT5 wafer A (100 ohm)	18	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	V
IT5 wafer B (100 ohm)	17	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	U
IT5 wafer A (100 ohm)	16	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	T
IT5 wafer B (100 ohm)	15	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	R
IT5 wafer A (100 ohm)	14	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	P
IT5 wafer B (100 ohm)	13	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	N
IT5 wafer A (100 ohm)	12	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	M
IT5 wafer B (100 ohm)	11	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	L
IT5 wafer A (100 ohm)	10	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	K
IT5 wafer B (100 ohm)	9	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	J
IT5 wafer A (100 ohm)	8	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	H
IT5 wafer B (100 ohm)	7	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G
IT5 wafer A (100 ohm)	6	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G
IT5 wafer B (100 ohm)	5	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	F
IT5 wafer A (100 ohm)	4	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	E
IT5 wafer B (100 ohm)	3	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	D
IT5 wafer A (100 ohm)	2	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	C
IT5 wafer B (100 ohm)	1	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	B
		G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	A
		G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	G	P	G	N	X

IT5*D-200S-BGA(**) Pin assignment footprint for mating side

Symbols

G: GND, Power
P: Positive of differential pair
N: Negative of differential pair

8 (P, X, N) Twisted pair used for differential

8 (P, -, N) Non twisted pair used for differential

DRAWING NO.	EDC3-341399-01
PART NO.	IT5-200P-22H(03)
CODE NO.	CL636-1049-4-03