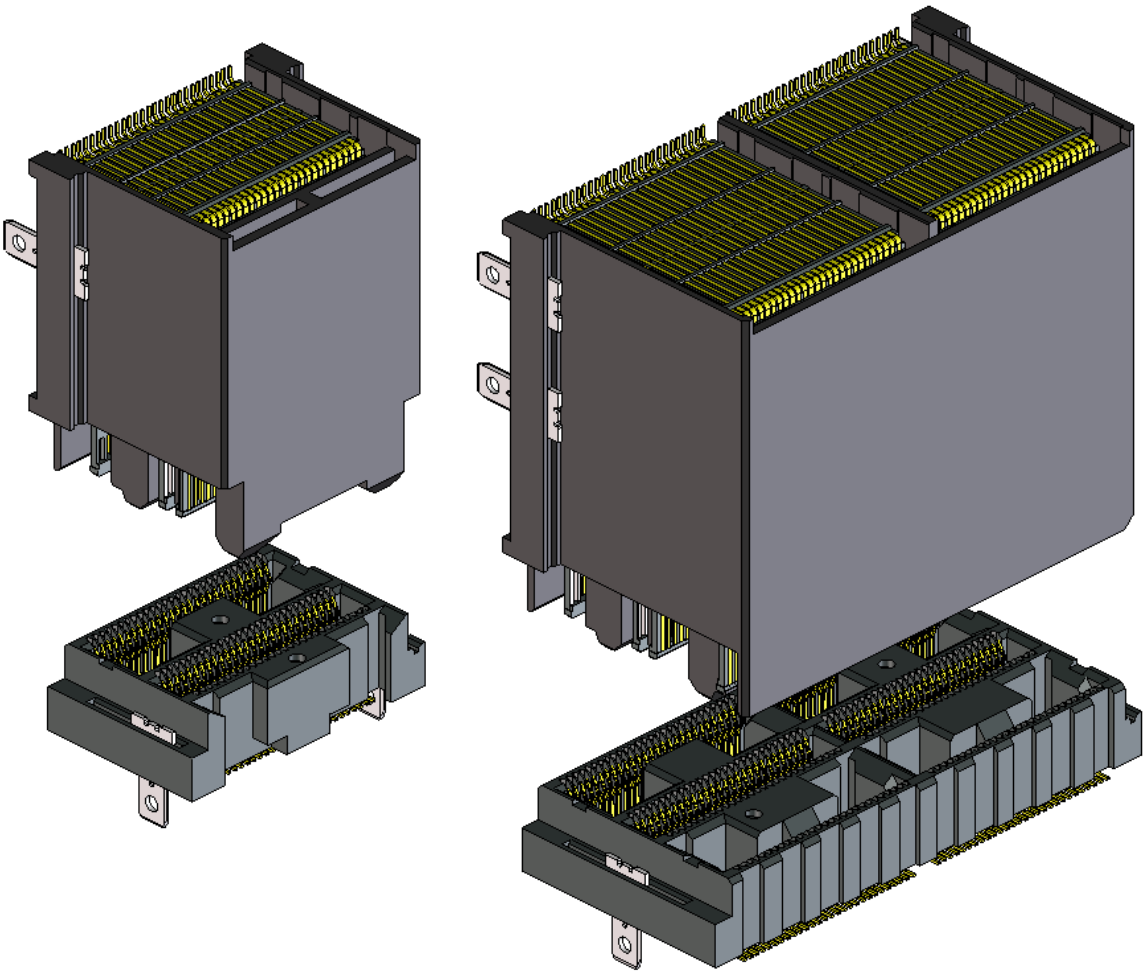
Hirose *IT9* ™

Connector System

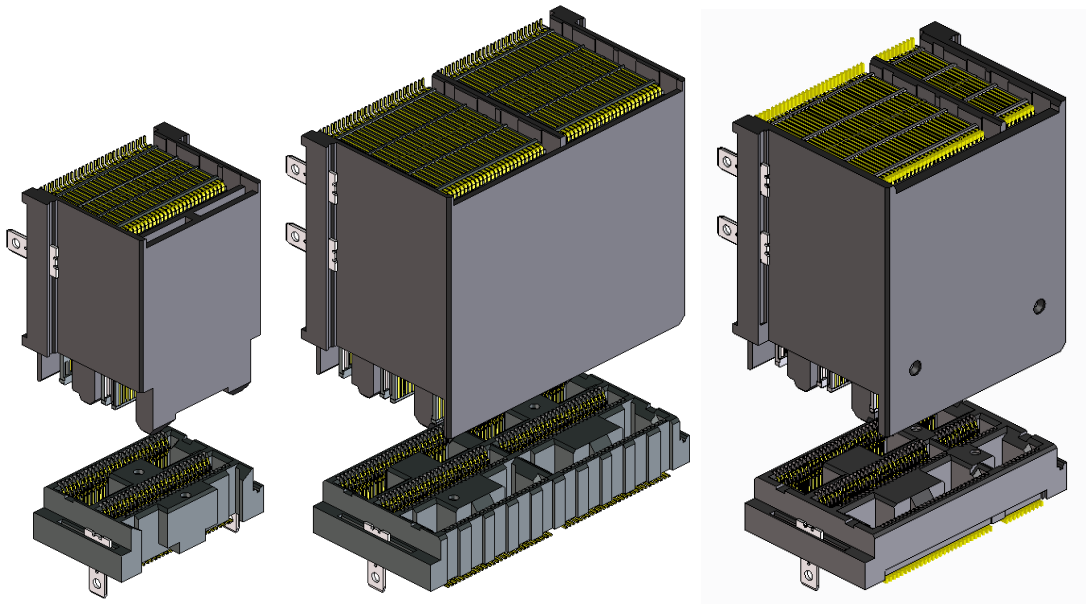
Design Notes



Revision No.	***Description (Major changes)***	***Date***
0.2	Draft	May.28th,2018
1.0	Initial release	Jun.25th,2018
2.0	Lot No. indication change Recommended Rework Condition Change	Jan.07th,2019
3.0	Added product info for M3 Added channel simulation result Updated SI result	May.18th,2021

Section 1 Introduction

*The Hirose **IT9** connector system is a two-piece type 3-row or 4-row SMT connector. Position counts of 84, 224 and 152 are available as standard variations. Please refer to individual product drawings for details.*



84 Pos. 224 Pos. 152 Pos.

Figure 1-1 Overview of IT9 Series

This section of the Design Note discusses the purpose, scope, and application and interpretation.

1.1 Purpose

*This technical bulletin is intended to provide basic information and product features of the Hirose **IT9** SMT connector system. By providing this information, Hirose believes it can help its customers to speed product development, improve quality and reliability, and limit overall system costs.*

1.2 Scope

*This guideline provides information useful for applications using the **IT9** SMT connector system. It provides information pertaining to:*

a) General Information
b) Operating Characteristics
c) Signal Integrity Information
d) PWB Design Information
e) Stencil Printing Information
f) Pick and Place Information
g) Reflow Processing Information
h) Assembly Processing Information

This document will be updated by Hirose as required to reflect current technologies and manufacturing capabilities. Please refer to individual product drawings for details.

1.3 Application and Interpretation

*This technical bulletin is intended to offer only general guidance and design concepts to customers. It does not limit customer designs nor guarantee results under all situations. Development of actual designs is the responsibility of each customer. Customers should consult with Hirose regarding their specific application, when, or if, any questions arise relating to these guidelines. Use of this technical bulletin is at customer's sole risk. This bulletin is provided "AS IS" and without warranty of any kind and HIROSE **expressly disclaims all warranties, express or implied, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose. HIROSE does not warrant that the guidelines contained in this bulletin will meet any customer's requirements. Furthermore, HIROSE does not warrant or make any representations regarding the use or the results of the use of information contained in this bulletin in terms of correctness, accuracy, reliability, or otherwise. Under no circumstance shall HIROSE or its directors, officers, employees or agents be liable for any incidental, special or consequential damages (including damages for loss of business, loss of profits, business interruption, loss of business information and the like) arising out of the use of the information contained in this bulletin.***

Section 2 General Information

*Hirose's **IT9** connector system is designed to provide modular high-speed differential, single-ended and power transmission for vertical board connection.*

IT9 plug side connector is built up with two types of blades- differential signal blades and power and low speed signal blades. Differential blades consist of ground plate and signal contacts, and each signal pairs are surrounded by ground.

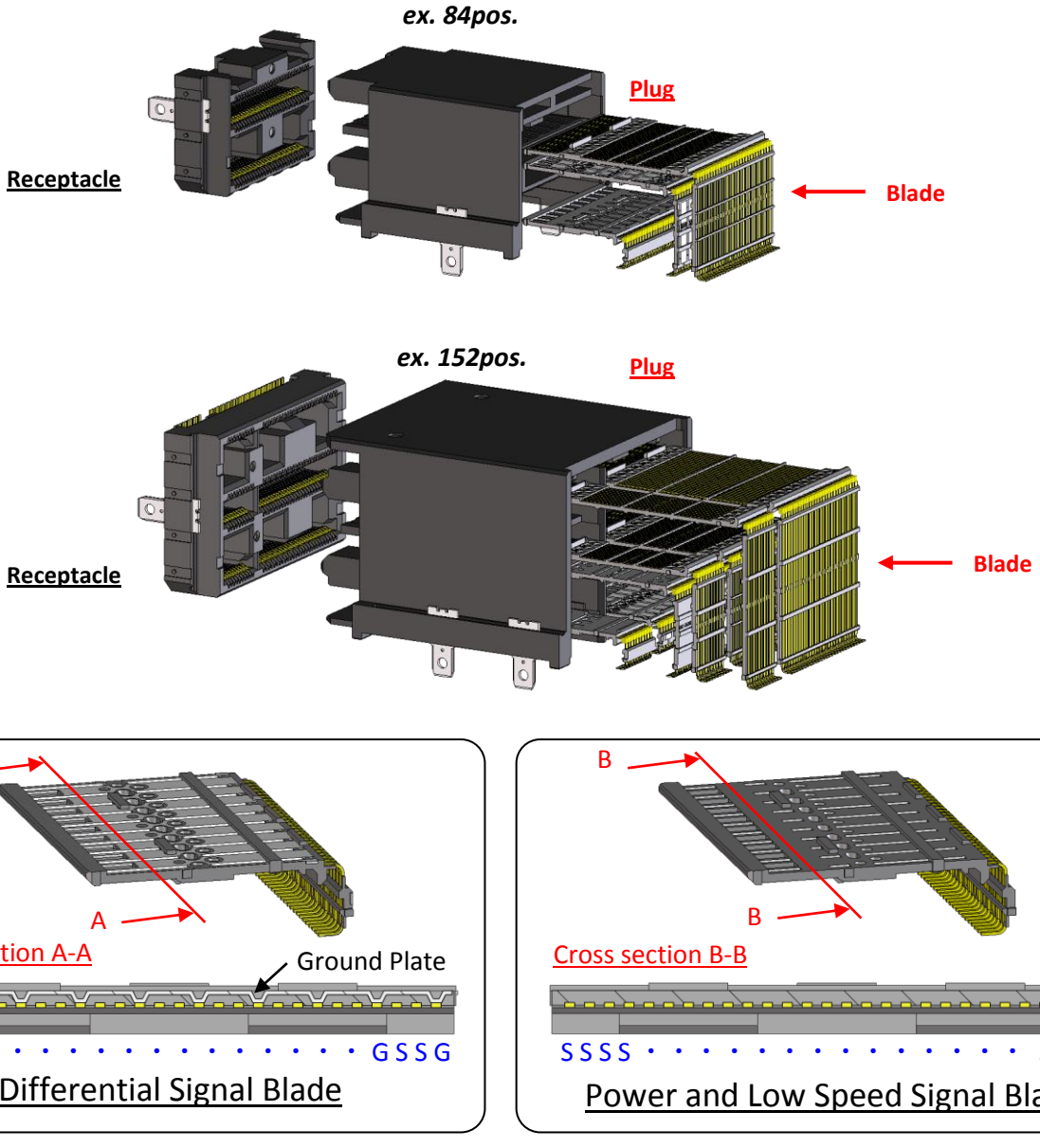


Figure 2-1 General Information

This section discusses part number designation, position count variations, component weights, manufacturing lot number, and general dimensions.

2.1 Part Number Designation / Contact Position Count Variations

2.1.1 Part Number Designation

Table 2-1 Part Number Designation

Plug Side	Receptacle Side
IT9Mx - xP - 0.5SHx (xx)	IT9Mx - xS - 0.5SVx (xx)
(1) (2)(3) (4)(5)(6)(7)	(1) (2)(3) (4)(5)(6)(7)

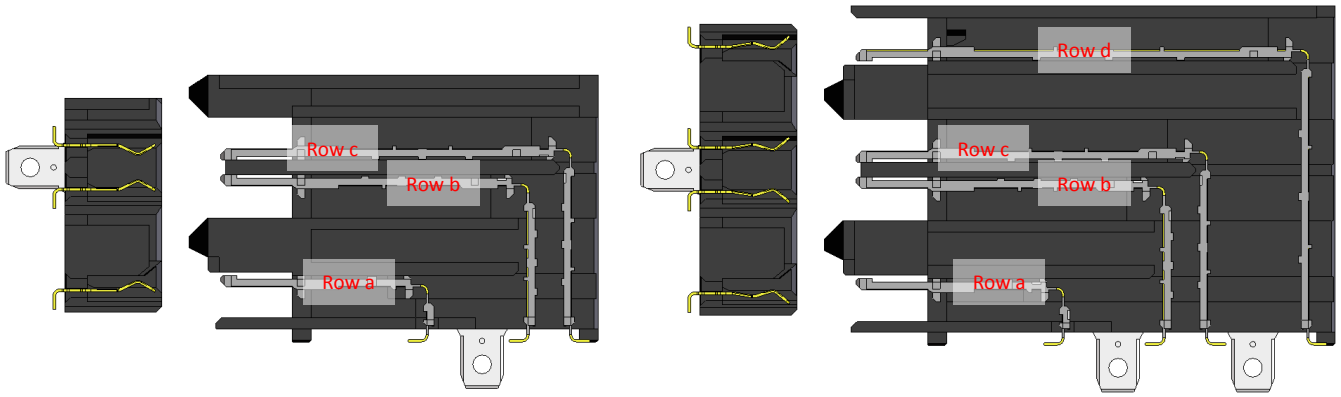
(1) Series name	
	2 : IT9M2 Series 3 : IT9M3 Series
(2) Contact Positions	
	84 : 84 pos. 224 : 224 pos. 152 : 152 pos.
(3) Connector Gender	
	P : Male (Plug) S : Female (Receptacle)
(4) Contact Pitch: 0.5	
	No Further Designation
(5) Contact Type	
	SH : Right Angle Type SV : Vertical Type
(6) Row Count	
	3 : 3 Rows (84 Pos. only) 4 : 4 Rows (224, 152 Pos.)
(7) Specification Number	
	Blank : Standard specification. See Table 2-3 for pin assignments. (xx) : Different options such as blade combination, plating, packaging, or customer specifics. Refer to individual drawings.

2.1.2 Contact Position Count Variations

Table 2-2 Contact Position Count Variations

Contact Positions	Plug	Receptacle
84	IT9M2-84P-0.5SH3 (**)	IT9M2-84S-0.5SV3 (**)
224	IT9M2-224P-0.5SH4 (**)	IT9M2-224S-0.5SV4 (**)
152	IT9M3-152P-0.5SH4 (**)	IT9M3-152S-0.5SV4 (**)

2.1.3 Pin Assignment



3 Rows Type *4 Rows Type*

Figure 2-2 Blade Row Identification

Table 2-3 Pin Assignment
<3 Rows Type>

Specification Number	Contact Positions	Column	Pin Number																										
			28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Any	84	Row c	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row b	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row a	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
		Row c : For High Speed Signal Row b : For High Speed Signal Row a : For Power and Low Speed Signal															S : Differential Signal Pin (36 Pins / 18 Pairs) G : Dedicated Ground Pin (20 Pins) U : Universal Pin (28 Pins)													

<4 Rows Type>

Specification Number	Contact Positions	Column	Pin Number																											
			28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Any	224	Row d	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
		Row c	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row b	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row a	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Column	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29
		Row d	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
		Row c	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row b	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row a	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G

Row d : For Power and Low Speed Signal
Row c : For High Speed Signal
Row b : For High Speed Signal
Row a : For High Speed Signal

S : Differential Signal Pin (108 Pins / 54 Pairs)
G : Dedicated Ground Pin (60 Pins)
U : Universal Pin (56 Pins)

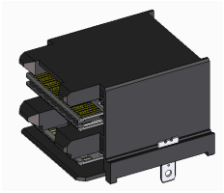
Specification Number	Contact Positions	Column	Pin Number																											
																					10	9	8	7	6	5	4	3	2	1
Any	152	Row d																			U	U	U	U	U	U	U	U	U	U
		Row c																			U	U	U	U	U	U	U	U	U	U
		Row b																			U	U	U	U	U	U	U	U	U	U
		Row a																			U	U	U	U	U	U	U	U	U	U
		Column	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11
		Row d	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row c	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row b	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G
		Row a	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G	S	S	G

1 to 10 Pin : For Power and Low Speed Signal
11 to 38 Pin : For High Speed Signal

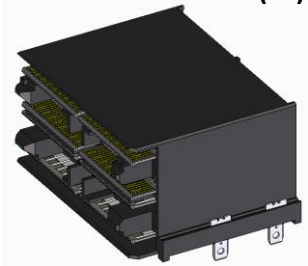
S : Differential Signal Pin (72 Pins / 36 Pairs)
G : Dedicated Ground Pin (40 Pins)
U : Universal Pin (40 Pins)

2.2 Component Weights

***ex. IT9M2-84P-0.5SH3* (**)**

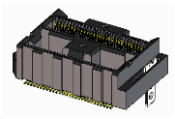


***ex. IT9M2-224P-0.5SH4* (**)**

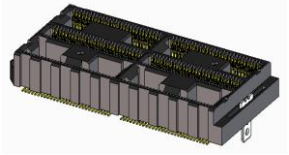


***ex. IT9M3-152P-0.5SH4* (**)**

***ex. IT9M2-84S-0.5SV3* (**)**



***ex. IT9M2-224S-0.5SV4* (**)**



***ex. IT9M3-152S-0.5SV4* (**)**

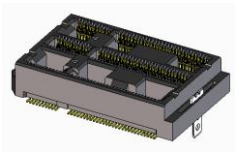
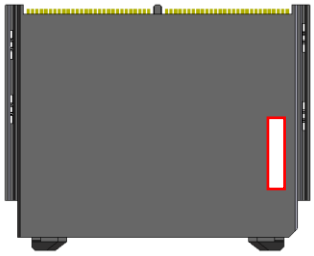


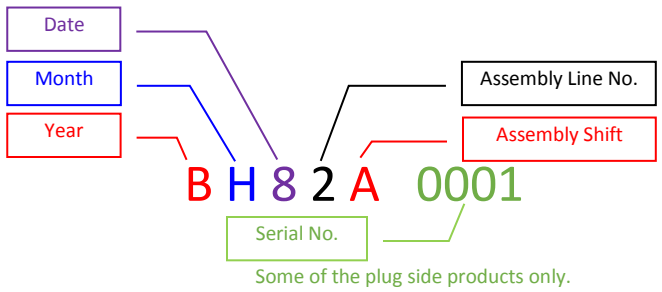
Table 2-4 Component Weight

Contact Positions	Part Number	Weight (g)
84	IT9M2-84P-0.5SH3(**)	3.7
	IT9M2-84S-0.5SV3(**)	1.0
224	IT9M2-224P-0.5SH4(**)	9.8
	IT9M2-224S-0.5SV4(**)	2.3
152	IT9M3-152P-0.5SH4(**)	8.9
	IT9M3-152S-0.5SV4(**)	1.9

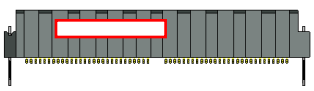
2.3 Manufacturing Lot Number

ex. Plug





* Lot number indication may be subject to change.



ex. Receptacle

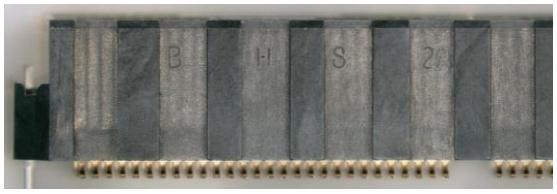


Figure 2-3 Indication

2.4 General Dimensions

Plug / Receptacle Outline

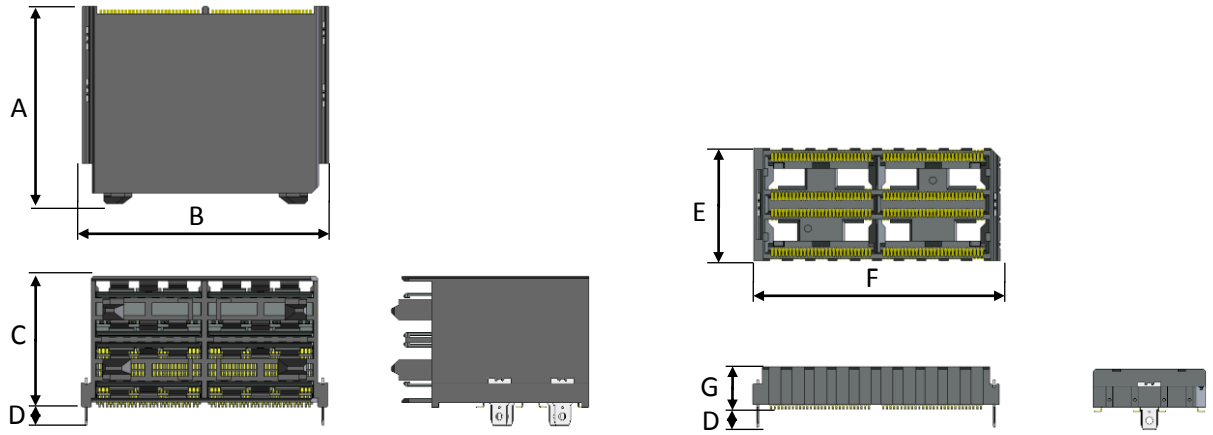


Table 2-5 General Dimensions

		Unit	Contact Positions		
			84	224	152
A	Plug outline length	mm	21.88	27.28	27.78
B	Plug outline width	mm	18.55	34.05	26.05
C	Plug height (from SMT lead)	mm	14.3	18.1	18.6
D	Retention peg length (from SMT lead)	mm	2.5		
E	Receptacle outline length	mm	11.47	15.5	15.5
F	Receptacle outline width	mm	18.55	34.05	26.05
G	Receptacle height (from SMT lead)	mm	5.84		

Please refer to individual product drawings for details.

Section 3 Operating Characteristics

This section discusses material, electrical, mechanical, and environmental characteristics.

3.1 Material

Numbering of component is same as customer drawing.

3.1.1 Plug

Table 3-1 Plug Material and Finish

No.	Component	Material	Finish & Remarks
1	Housing	LCP	Black , UL 94V-0
2	Contact	Copper Alloy	Contact Area : Gold (0.76µm min) over Nickel (3.0µm min) Mount Area : Gold (0.03µm min) over Nickel (1.0µm min)
3	Blade	LCP	Black , UL 94V-0
4	Ground Plate	Stainless Steel	-
5	Retention Peg	Copper Alloy	Sn (3.0µm min) over Nickel (1.0µm min)
6	Hard Tray	HIPS	Black
7	Top Cover	HIPS	Black

3.1.2 Receptacle

Table 3-2 Receptacle Material and Finish

No.	Component	Material	Finish & Remarks
1	Housing	LCP	Black , UL 94V-0
2	Contact	Copper Alloy	Contact Area : Gold (0.76µm min) over Nickel (3.0µm min) Mount Area : Gold (0.03µm min) over Nickel (1.0µm min)
3	Retention Peg	Copper Alloy	Sn (3.0µm min) over Nickel (1.0µm min)
4	Pick Up Tape	Nomex	-
5	Embossed Carrier Tape	PS	-
6	Top Cover Tape	PS	-

3.2 Electrical

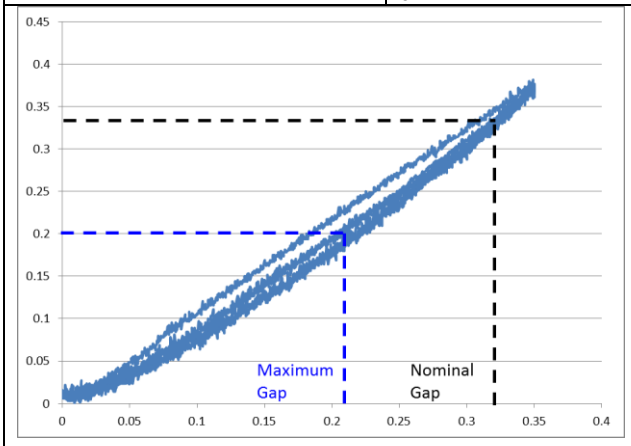
Table 3-3 Electrical Test Conditions and Requirements

Test	Test Condition	Requirement	Typical Value
Low Level Contact Resistance* (LLCR)	EIA-364-23	60mΩ max (*1) (Row A) 70mΩ max (*1) (Row B) 80mΩ max (*1) (Row C) 90mΩ max (*1) (Row D)	Ex. 224pos. (Row A) 27.0mΩ (Row B) 42.0mΩ (Row C) 45.6mΩ (Row D) 64.8mΩ
Insulation Resistance (IR)	EIA-364-21	100MΩ min	Ex. 224pos. 2.00E+05MΩ
Dielectric Withstanding Voltage (DWV)	EIA-364-20 AC 150V for 60 seconds	No flashover or breakdown	Ex. 224pos. No flashover or dielectric breakdown was found

* The value of contact resistance includes contact point and the bulk resistance.

3.3 Mechanical

Table 3-4 Mechanical Test Conditions and Requirements

Test	Test Condition	Requirement	Typical Value
Insertion / Withdrawal Force	EIA-364-13	Insertion Force : 0.4 N/pin max Withdrawal Force : 0.015 N/pin max	Ex. 84pos. IF/WF : 21.2/10.3N Ex. 224pos. IF/WF : 58.6/31.1N
Mechanical Operation	EIA-364-09 Cycle rate: 300 max per hour 100 times	1) Contact resistance change : 10mΩ or less 2) No damage, crack, or looseness of parts	Ex. 224pos. (Row A) <+10mΩ (Row B) <+10mΩ (Row C) <+10mΩ (Row D) <+10mΩ
Random Vibration	EIA-364-28 Frequency:20 TO 500Hz Power Special Density:0.02G²/Hz for 60 min in 3 directions	1) No electrical discontinuity of 1 μs or more 2) No damage, crack, or looseness of parts	No electrical discontinuity of 1 μs or more was found. No damage, crack, or looseness of parts were found
Packing	ISTA-3A	No evidence of physical damage SMT Coplanarity : 0.13mm max	Ex. 224pos. No evidence of physical damage was found. SMT Coplanarity : <0.13mm
Contact Normal Force	-	0.2N min	0.45N
			Ex. IT9M2-224S-0.5SV4
Contact Wiping Length	IT9M2 Series : 2.0 +/-0.3 mm IT9M3 Series : 1.5 +/-0.3 mm		-
Retention Force	0.5N min / Signal contact 2.0N min / Retention peg		Ex.224pos.Receptacle Signal contact : 2.78N Retention peg : 8.82N
SMT Coplanarity	0.13 mm max		-

3.4 Environmental

*Based on accelerated high temperature tests that store connectors at 105 °C for more than 120 hours according to EIA-364-1000.01, the **IT9** can be stored for up to 10 years. Refer to Table 3-5 for the environmental standards and conditions that the **IT9** has been tested to meet.*

*The **IT9** has been tested and meets the requirements for environmentally-related corrosive atmosphere according to EIA-364-65. These test procedures demonstrate how plated and unplated surfaces react when exposed to different concentrations of flowing gas mixtures.*

Table 3-5 Environmental Test Conditions and Requirements

Test	Test Condition	Requirement	Remarks
Thermal Shock	EIA-364-32 Condition I Temperature (°C): -55 →20 ~ 35 → 85 →20 ~ 35 Time (min): 30 → 5 max → 30 → 5 max Under 10 cycles	1) Contact resistance change: +10mΩ or less 2) No damage, crack, or looseness of parts	-
Cyclic Temperature & Humidity	EIA-364-31 @ 25°C, 90~95% RH:120 min Dwell time ↓ 120 min Ramp time @ 65°C , 90~95% RH:120 min Dwell time Under 60 cycles	1) Contact resistance change: +10mΩ or less 2) No damage, crack, or looseness of parts	-
Dry Heat	EIA-364-17 Exposed at 105 °C, 300h	1) Contact resistance change: +10mΩ or less 2) No damage, crack, or looseness of parts	-
Mixed Flowing Gas	EIA-364-65 Exposed at 30°C, 70% RH Cl_2: 10ppb, NO_2: 200ppb, H_2S: 10ppb, SO_2: 100ppb Mated 10 days	1) Contact resistance change: +10mΩ or less 2) No heavy corrosion	-
Dust	EIA-364-91 Unmated 1 hour	Contact resistance change: +10mΩ or less	-

Section 4 Signal Integrity Information

*This section contains the overview, 32 Gbps solution, differential performance, a full-channel simulation of a PCIe environment using, and propagation delay of Hirose's **IT9** signal integrity performance, as well as an introduction of Hirose's patented FEXT cancellation via structure.*

4.1 Overview

The IT9 minimizes signal loss and crosstalk by adopting a unique enhanced GND design (Figure 2-1).
As a result, IT9 is able to meet the stringent (enhanced) insertion loss-to-crosstalk ratio (ICR) specifications specified in IEEE802.3ap up to 16GHz (=32Gbps).

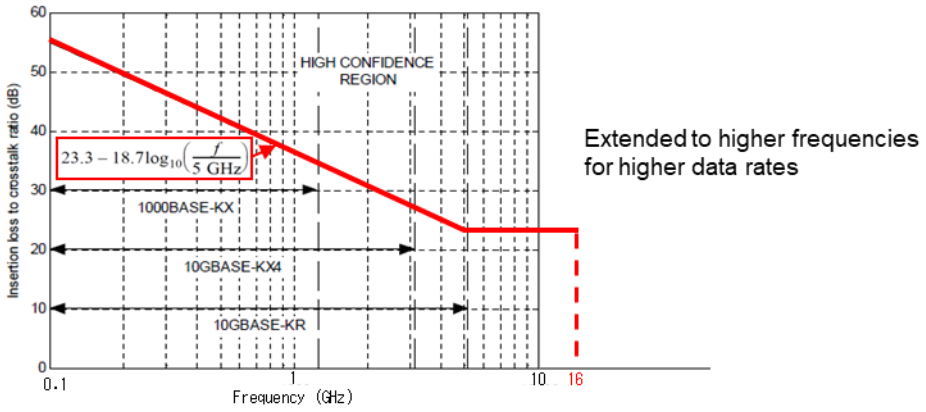


Figure 4-1 ICR Specification

<IT9M2 Series>

Actual measurements were taken with IT9M2-84P[1] and 84S connectors, transitions through outer routing layers, and micro strip traces de-embedded (Figure 4-2).

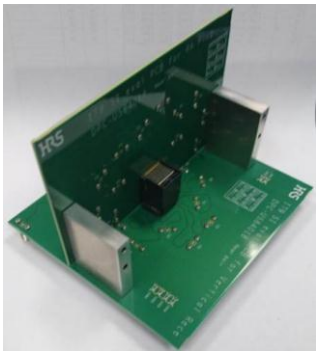


Figure 4-2 SI Test board

[1] *Row-a modified to differential signal blade for measurement*

The following ICR curves correspond to the power sum of NEXT[2] (Figure 4-3) and FEXT[3](Figure 4-4) from 8 aggressor pairs and 1 victim pair in 3 columns of IT9-84P/S. It is clear that ***IT9M2*** *meets the ICR spec. for 32 Gbps data rate in a populated configuration (Figure 4-5).*

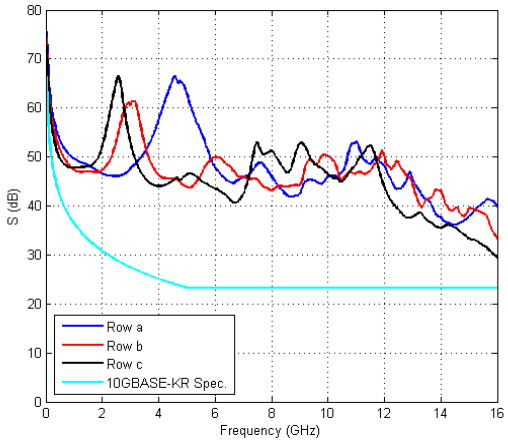


Figure 4-3 ICR with 8 NEXT

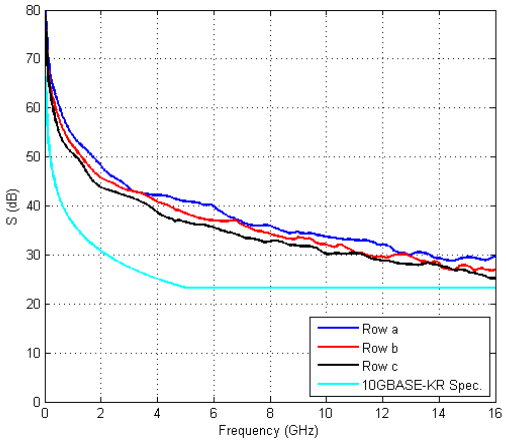


Figure 4-4 ICR with 8 FEXT

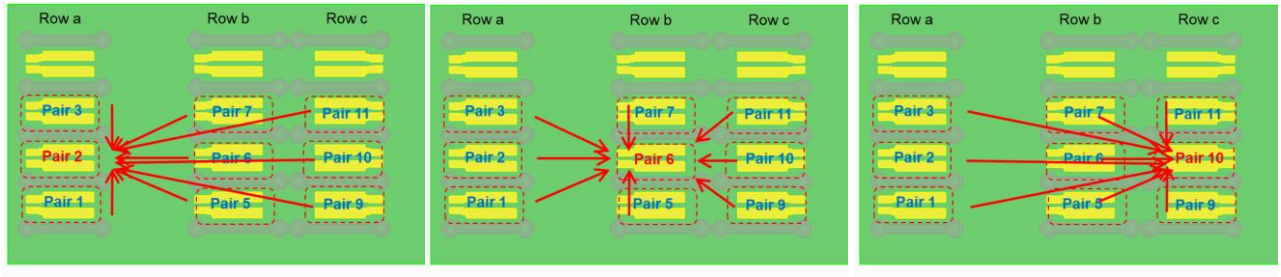


Figure 4-5 Populated Pin Configuration

<IT9M3 Series>

Actual measurements were taken on test boards with IT9M3-152P and 152S connectors, transitions through surface layer, and coplanar traces de-embedded. (Figure 4-6)

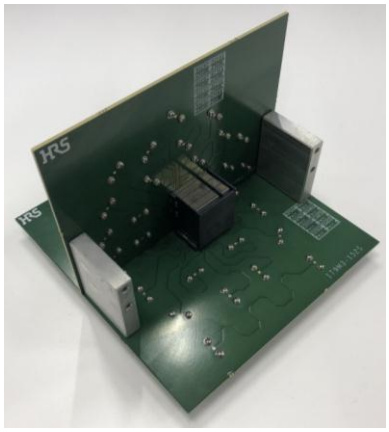


Figure 4-6 SI Test board

[2] *near-end crosstalk*

[3] *far-end crosstalk*

*The following ICR curves correspond to the power sum of near-end crosstalk (Figure 4-7) and far-end crosstalk (Figure 4-8) from 11 aggressor pairs and 1 victim pair in 4 columns of IT9-152P/S. It is clear that **IT9M3** meets the ICR spec. for 32 Gbps data rate in a populated configuration (Figure 4-9).*

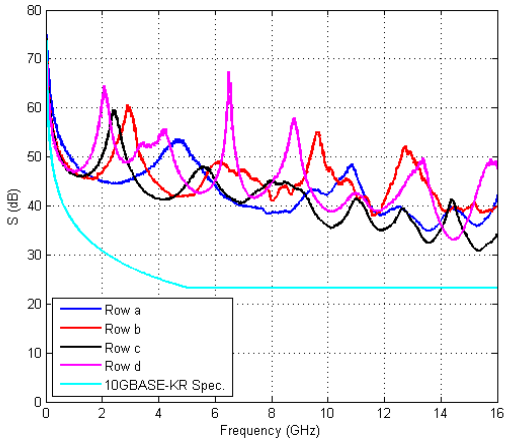


Figure 4-7 ICR with 11 NEXT

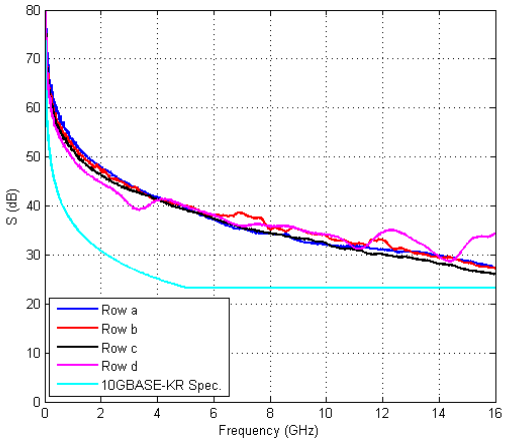


Figure 4-8 ICR with 11 FEXT

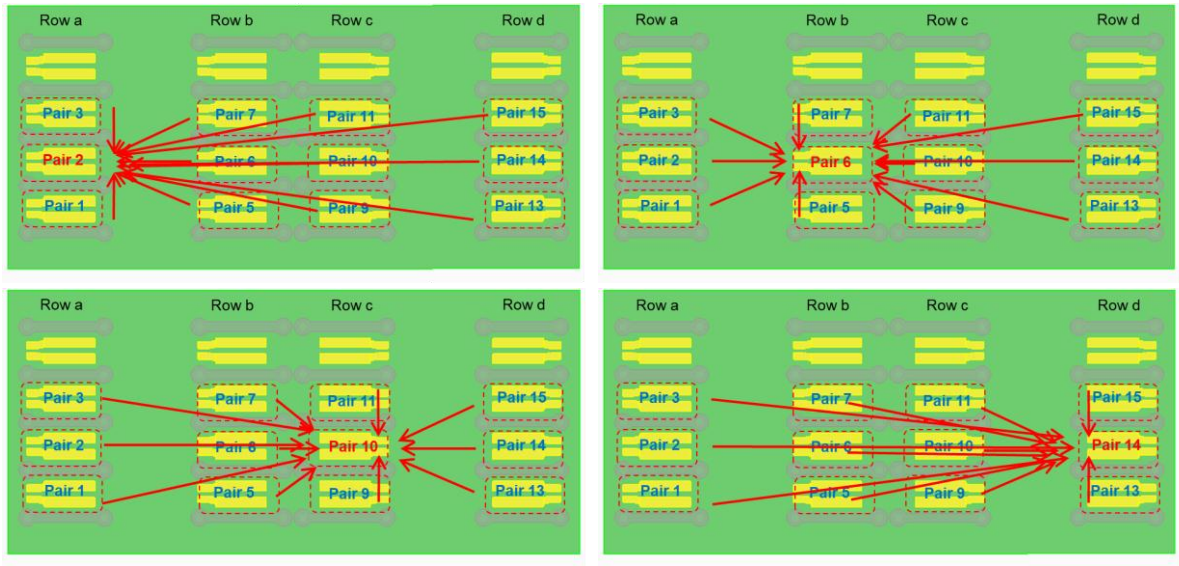


Figure 4-9 Populated Pin Configuration

4.2 Differential Signals

<IT9M2 Series>

Figures 4-11 to 4-14 show the measured differential insertion loss (IL), return loss (RL), NEXT, and FEXT between two nearest neighbors for each row (Figure 4-10).

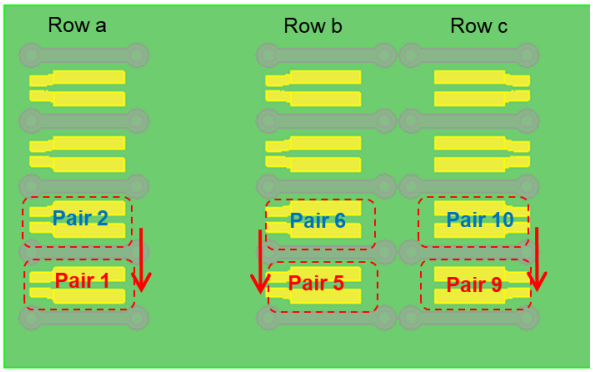


Figure 4-10 Nearest neighbors of IT9M2

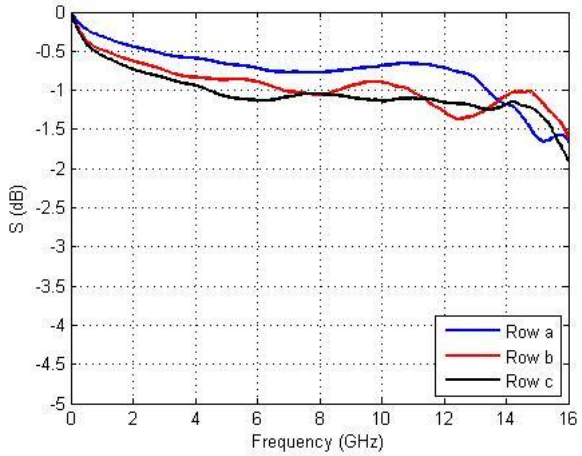


Figure 4-11 Differential IL of IT9M2

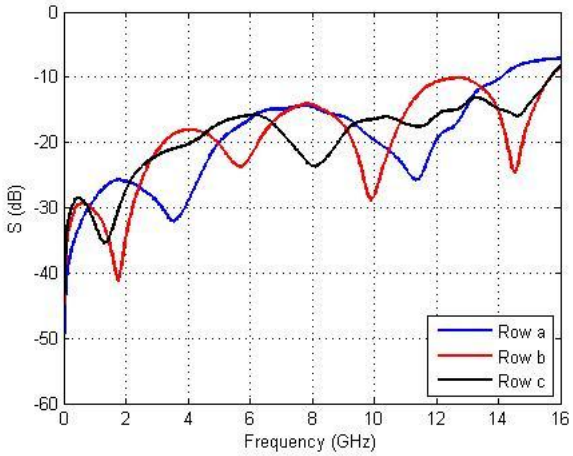


Figure 4-12 Differential RL of IT9M2

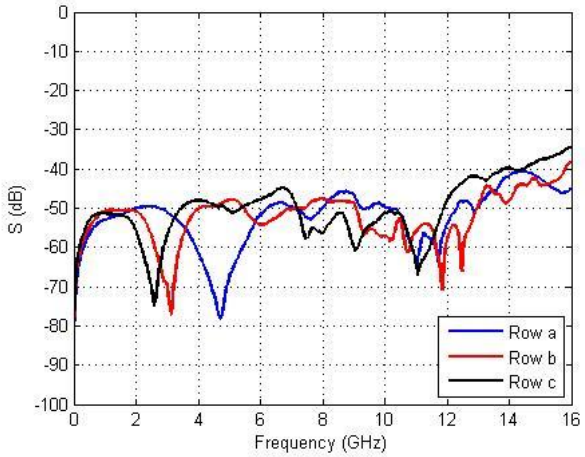


Figure 4-13 Differential NEXT of IT9M2

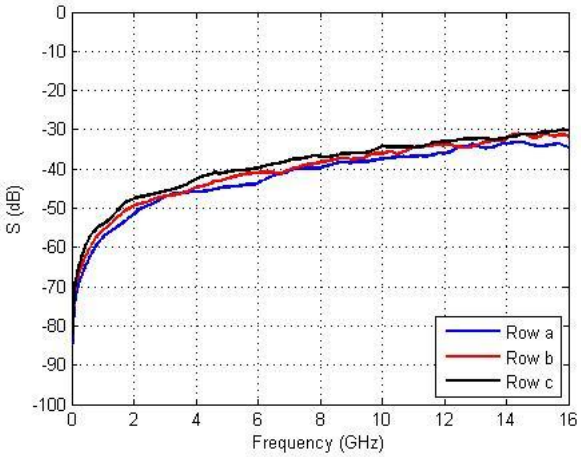


Figure 4-14 Differential FEXT of IT9M2

Figures 4-15 to 4-19 show the measured vs. simulated differential IL, RL, NEXT, FEXT between two nearest neighbors in Row a, and impedance.

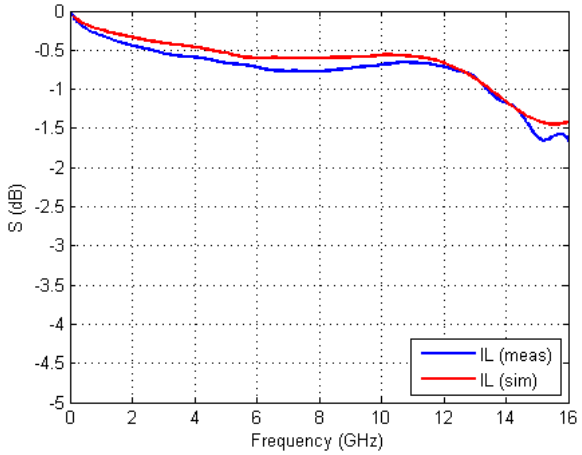


Figure 4-15 Differential IL of IT9M2

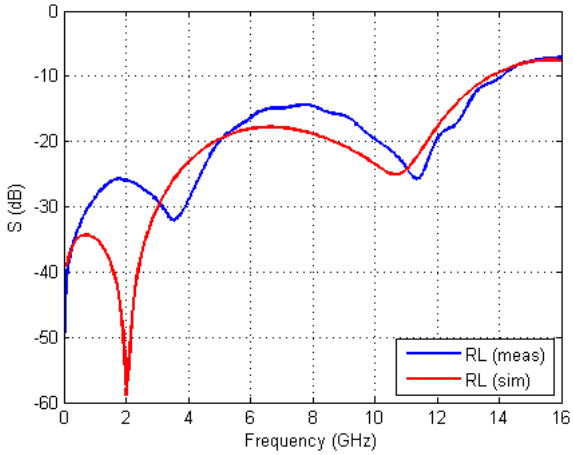


Figure 4-16 Differential RL of IT9M2

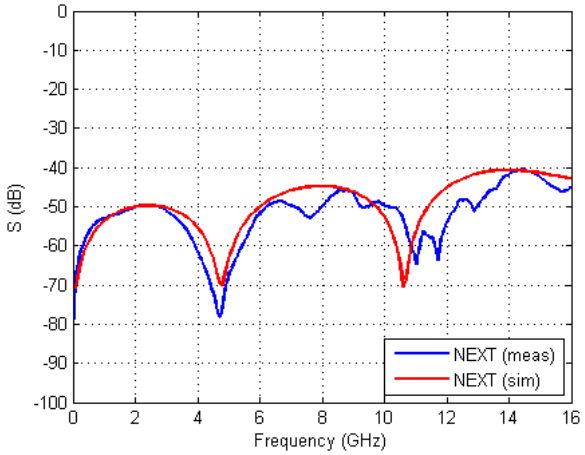


Figure 4-17 Differential NEXT of IT9M2

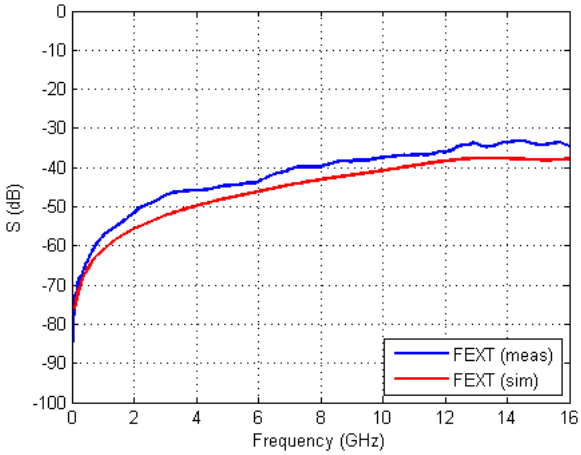


Figure 4-18 Differential FEXT of IT9M2

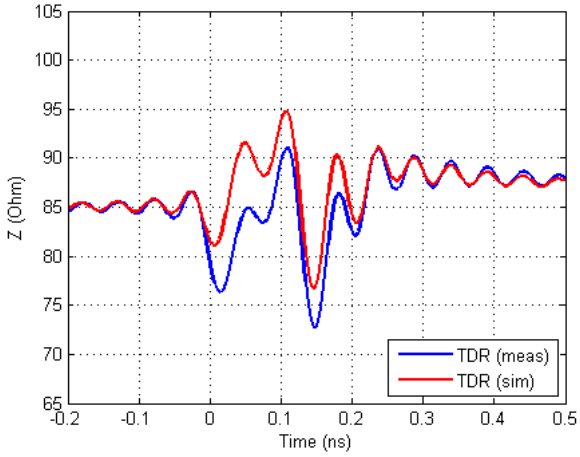


Figure 4-19 Differential Impedance (rise time=12.5ps)

Figures 4-21 to 4-24 show the measured differential IL, RL, NEXT, FEXT between two nearest neighbors for each row (Figure 4-20).

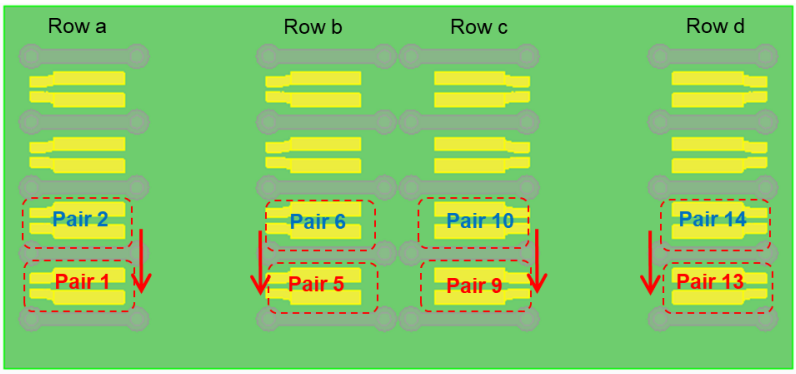


Figure 4-20 Nearest neighbors of IT9M3

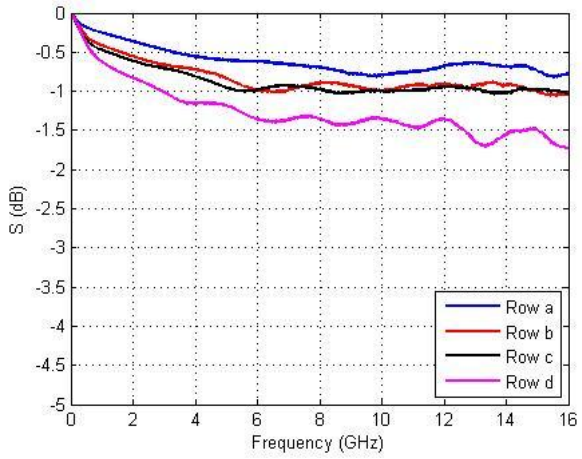


Figure 4-21 Differential IL of IT9M3

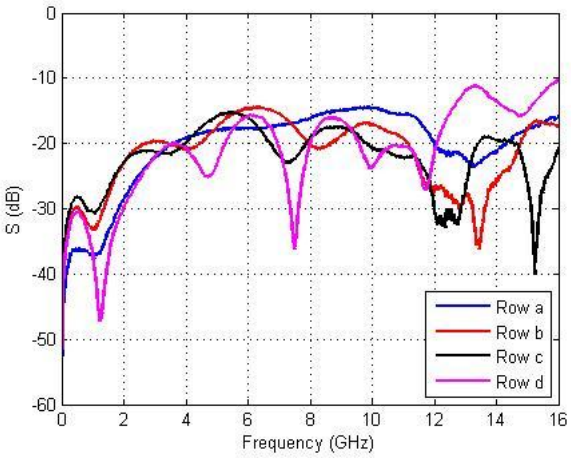


Figure 4-22 Differential RL of IT9M3

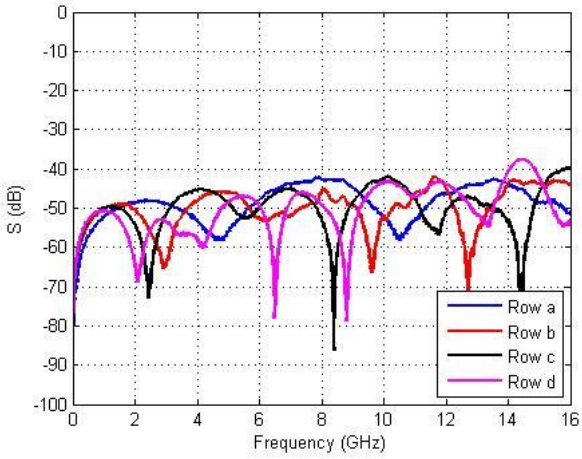


Figure 4-23 Differential NEXT of IT9M3

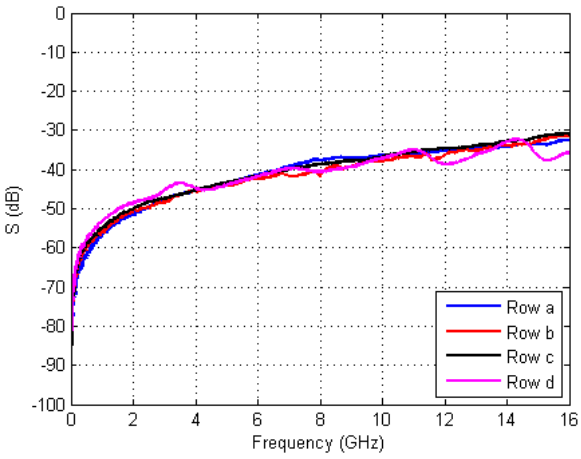


Figure 4-24 Differential FEXT of IT9M3

Figures 4-25 to 4-29 show the measured vs. simulated differential IL, RL, NEXT, FEXT between two nearest neighbors in Row a, and impedance.

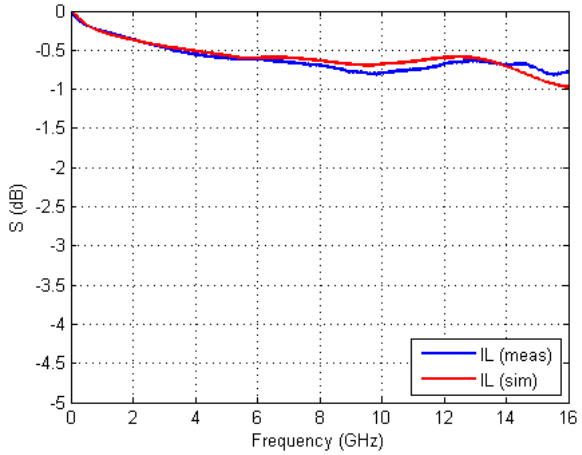


Figure 4-25 Differential IL of IT9M3

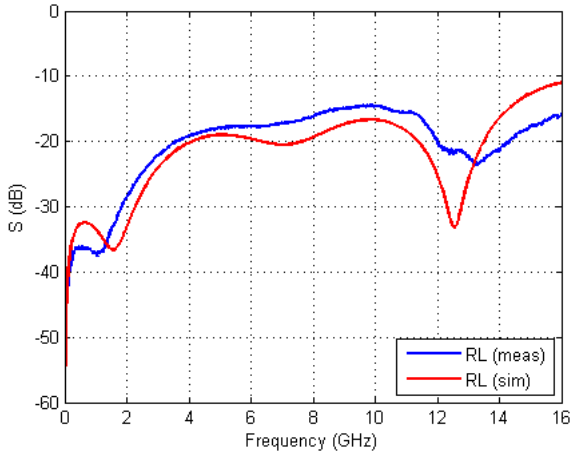


Figure 4-26 Differential RL of IT9M3

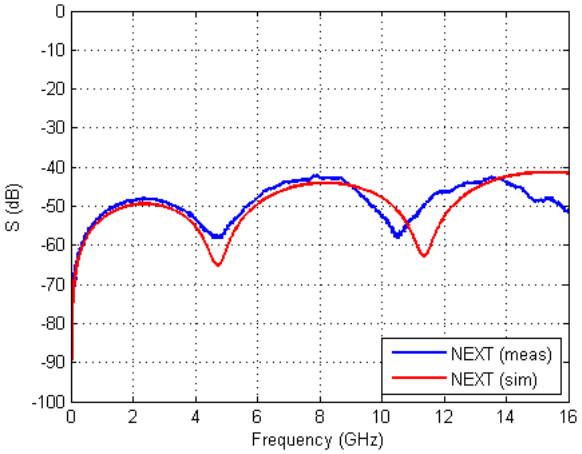


Figure 4-27 Differential NEXT of IT9M3

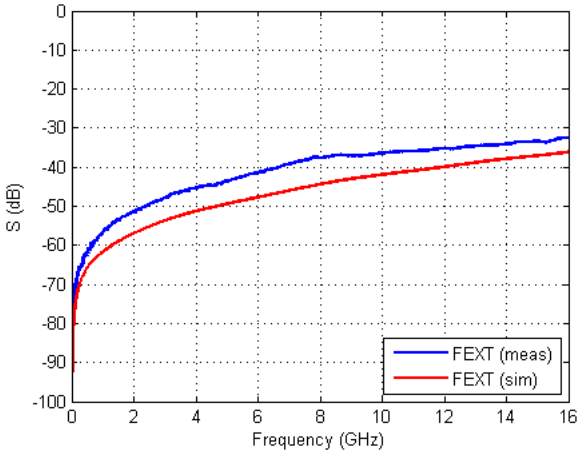


Figure 4-28 Differential FEXT of IT9M3

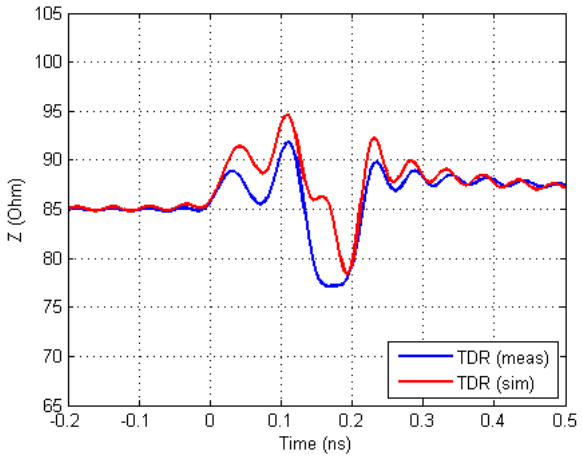


Figure 4-29 Differential Impedance (rise time=12.5ps)

4.3 PCIe Channel Example

4.3.1 Overview

This section will demonstrate the feasibility of IT9's use within a PCIe Gen4 and 5 environment through full-channel simulations using Seasim Ver.0.78. A one-connector topology was examined, with the focus being on just the Row C and Row D channels for IT9M2 and IT9M3 respectively (Figure 4-30) for the sake of brevity, based on the assumption that longer channels will have higher loss thus smaller eye openings.

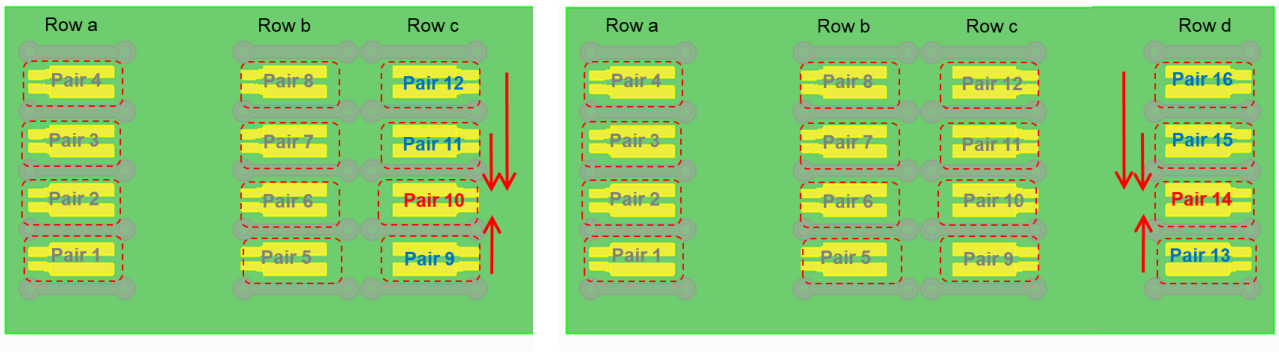
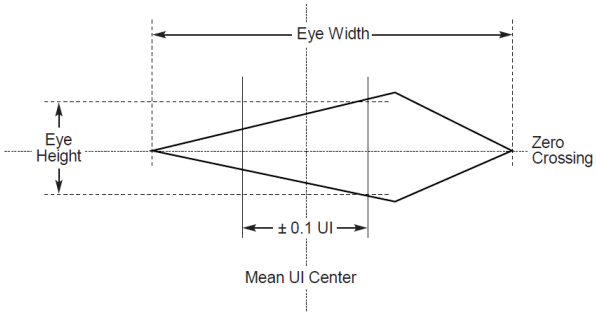


Figure 4-30 Each row examined with three aggressors from the same row (left: IT9M2, right: IT9M3)

4.3.2 PCIe4.0/5.0 Compliance Specification

Section 8.5.1.4.3 of the PCI Express Base Specification, Rev. 5.0, Version 1.0 characterizes the pass/fail of a channel with the following eye mask (Figure 4-31), with the minimum compliance limit of the eye height defined as 15mVpp and the eye width as 0.3UI for both Gen4 and 5

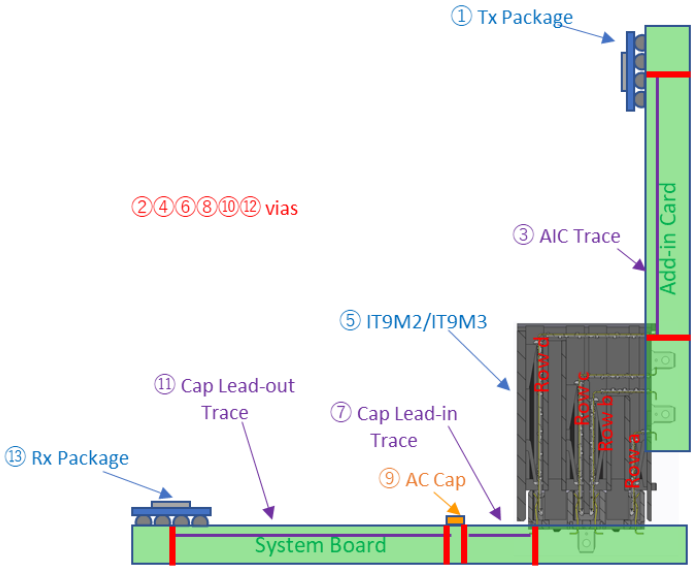


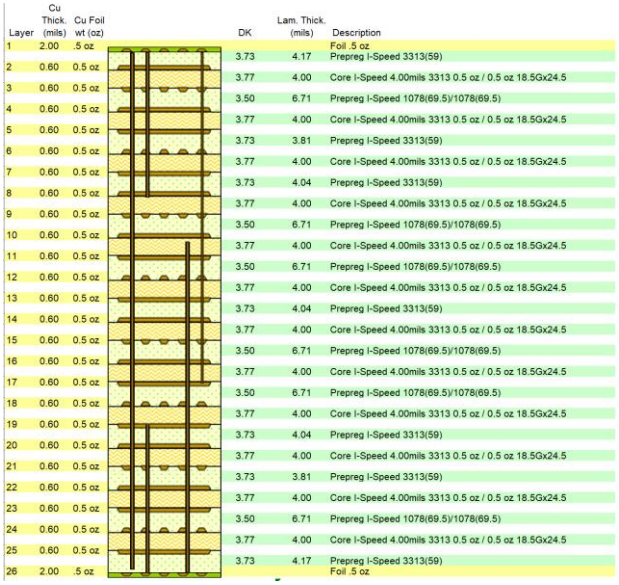
Eye height	15mV (Min)
Eye width at zero crossing	0.3UI (Min)

Figure 4-31 Pass/Fail eye mask as defined in PCIe 4.0/ 5.0 Base Specification (pg 1082-1084)

4.3.3 Channel Simulation

As an examination of the feasibility of IT9 application within a PCIe4.0/5.0 channel, full-channel simulation models were created following the topology seen in Figure 4-32. Included components follow the loss curves shown in Figure 4-33 to fit within the loss budgets proposed by the PCI-Sig work group. Both the PCIe4.0 and 5.0 simulation models refer to the stack-up shown in Figure 4-33 at both the System Board and Add-in Card, with FEXT-cancellation vias (see Section 4.5) going from L1 to L24. The resulting eye diagrams produced through Seasim simulation (Figure 4-36 and 4-37) were examined with 3 aggressors as seen in Figure 4-30 and the adapt/equalizer configuration seen in Figures 4-34 and 4-35.





Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	2.00	.5 oz			Foil .5 oz
2	0.60	0.5 oz	3.73	4.17	Prepreg I-Speed 3313(59)
3	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
4	0.60	0.5 oz	3.50	6.71	Prepreg I-Speed 1078(69.5)/1078(69.5)
5	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
6	0.60	0.5 oz	3.73	3.81	Prepreg I-Speed 3313(59)
7	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
8	0.60	0.5 oz	3.73	4.04	Prepreg I-Speed 3313(59)
9	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
10	0.60	0.5 oz	3.50	6.71	Prepreg I-Speed 1078(69.5)/1078(69.5)
11	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
12	0.60	0.5 oz	3.50	6.71	Prepreg I-Speed 1078(69.5)/1078(69.5)
13	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
14	0.60	0.5 oz	3.73	4.04	Prepreg I-Speed 3313(59)
15	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
16	0.60	0.5 oz	3.50	6.71	Prepreg I-Speed 1078(69.5)/1078(69.5)
17	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
18	0.60	0.5 oz	3.50	6.71	Prepreg I-Speed 1078(69.5)/1078(69.5)
19	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
20	0.60	0.5 oz	3.73	4.04	Prepreg I-Speed 3313(59)
21	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
22	0.60	0.5 oz	3.73	3.81	Prepreg I-Speed 3313(59)
23	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
24	0.60	0.5 oz	3.50	6.71	Prepreg I-Speed 1078(69.5)/1078(69.5)
25	0.60	0.5 oz	3.77	4.00	Core I-Speed 4.00mils 3313 0.5 oz / 0.5 oz 18.5Gx24.5
26	2.00	.5 oz	3.73	4.17	Prepreg I-Speed 3313(59)
					Foil .5 oz

Figure 4-32 High-level diagram for the 16.0GT/s and 32.0GT/s example channels (left). Both the System Board and AIC for the two channels follow the stack-up shown (right)

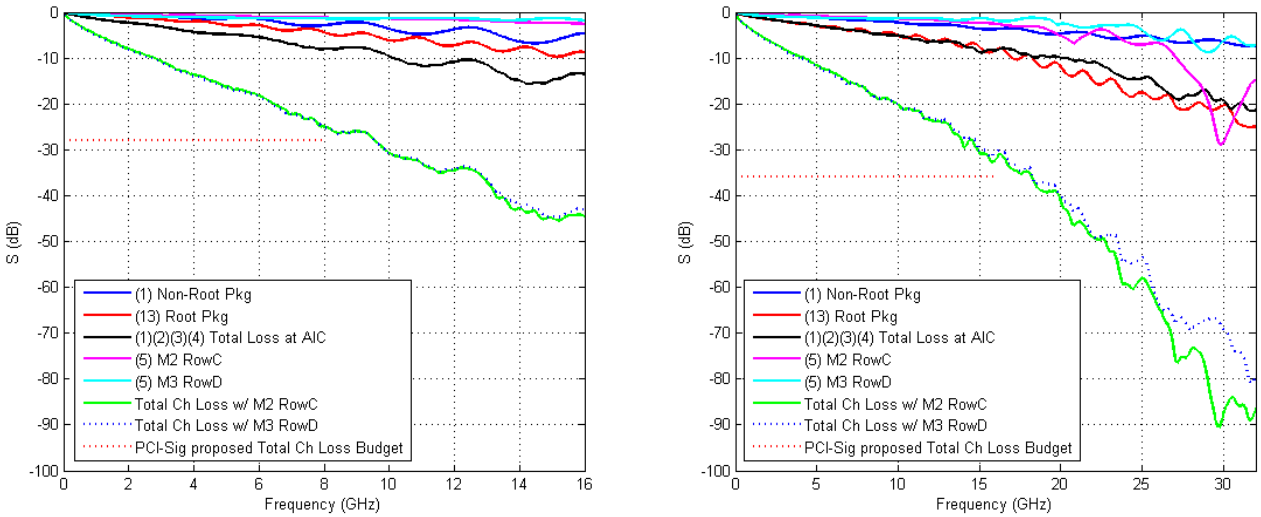


Figure 4-33 Components in the channel (left: for 16GT/s Gen4, right: for 32GT/s Gen5)

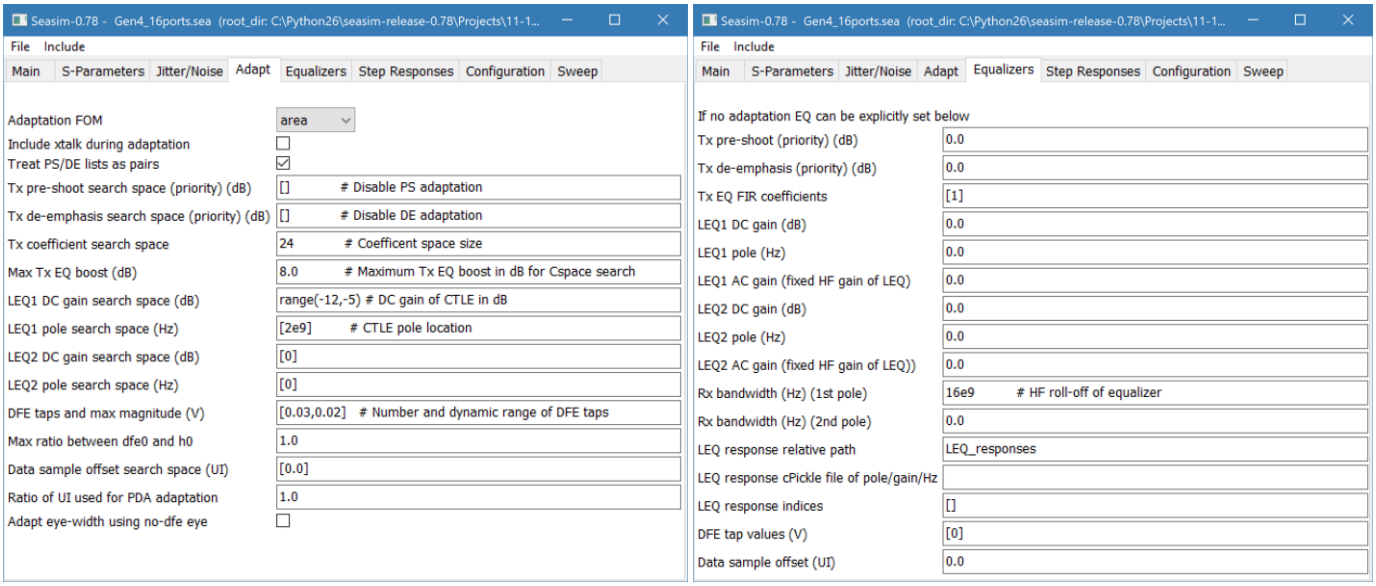


Figure 4-34 Seasim Adapt (left) and Equalizers (right) configurations for PCIe4.0 16GT/s simulation

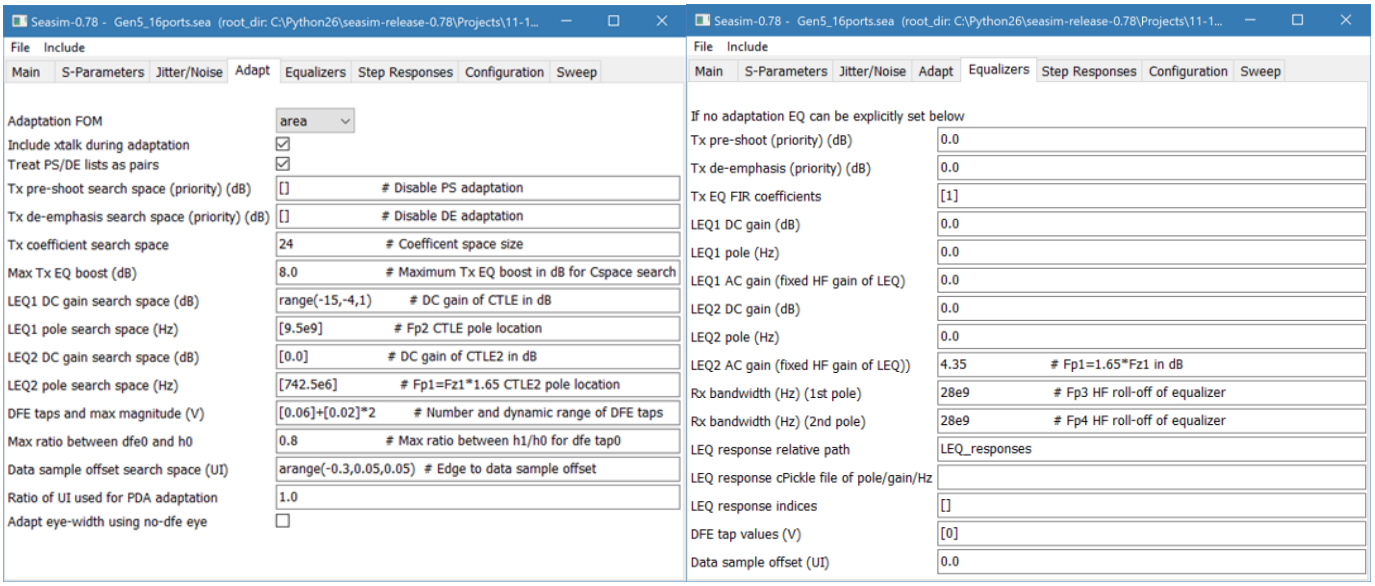
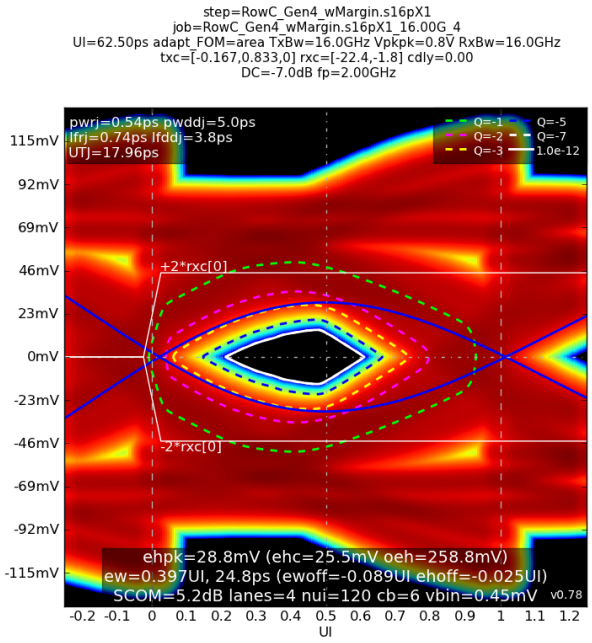
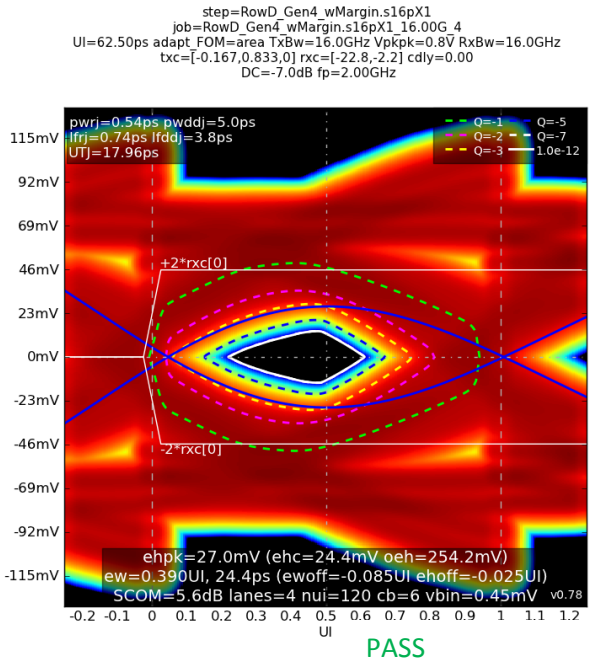


Figure 4-35 Seasim Adapt (left) and Equalizers (right) configurations for PCIe5.0 32GT/s simulation

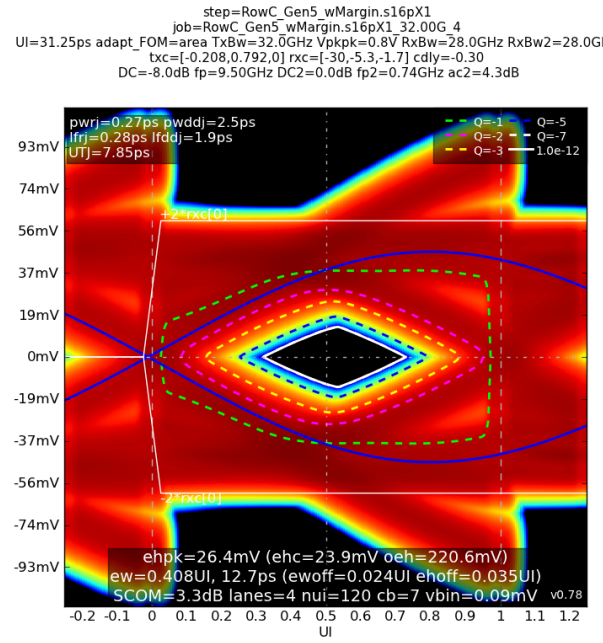


PASS
EH: 28.8mVpp
EW: 0.397UI

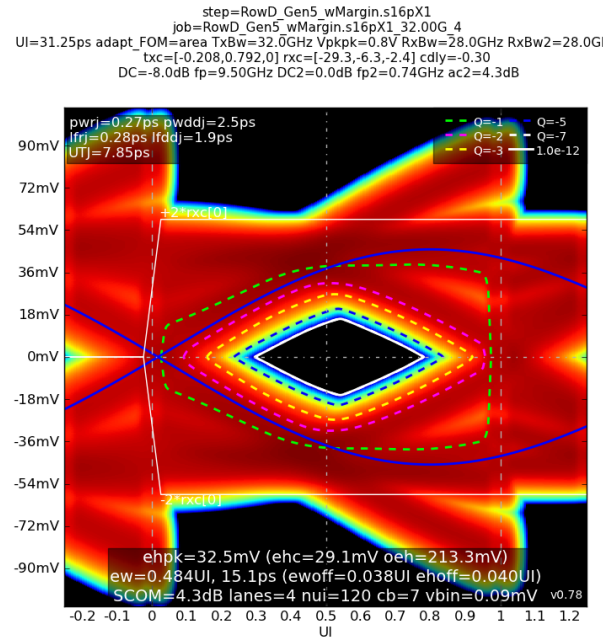


PASS
EH: 27.0mVpp
EW: 0.390UI

Figure 4-36 16GT/s Eye for channel incorporating IT9M2 RowC (left) and IT9M3 RowD (right)



PASS
EH: 26.4mVpp
EW: 0.408UI



PASS
EH: 32.5mVpp
EW: 0.484UI

Figure 4-37 32GT/s Eye for channel incorporating IT9M2 RowC (left) and IT9M3 RowD (right)

4.3.4 Comments on Feasibility

Through analysis of the channel simulation results observed in Section 4.3.3 of this document (summarized in Table 4-1 and Figure 4-38), it can be safely concluded that it is possible to adopt both IT9M2 and IT9M3 into working PCIe4.0 16.0 GT/s channel, as can also be said for PCIe5.0 32.0 GT/s channel. One trend that is of note however, is the slight variance in resulting eye between the channel with IT9M2 and IT9M3. At the 16GT/s simulation, the channel using IT9M2 Row C resulted in a larger eye than with IT9M3 Row D. This relationship is flipped for the 32GT/s simulation, where the simulation using IT9M3 Row D has the larger eye. This seems to be consistent with what is observed at the connector-only performance (Figure 4-39). Comparing the IL at IT9M2 Row C and IT9M3 Row D, it can be observed that at 8GHz, the fundamental frequency for PCIe4.0, Row D is more lossy, while at 16GHz, Row C ends up becoming more lossy.

	PCIe4.0 (16GT/s)		PCIe5.0 (32GT/s)	
	EH (mV_{pp})	EW (UI)	EH (mV_{pp})	EW (UI)
IT9M2 Series (Row C)	28.8	0.397	26.4	0.408
IT9M3 Series (Row D)	27.0	0.390	32.5	0.484

Table 4-1 Summary of Simulated Eye for example PCIe4.0 & PCIe5.0 channel for IT9M2/M3

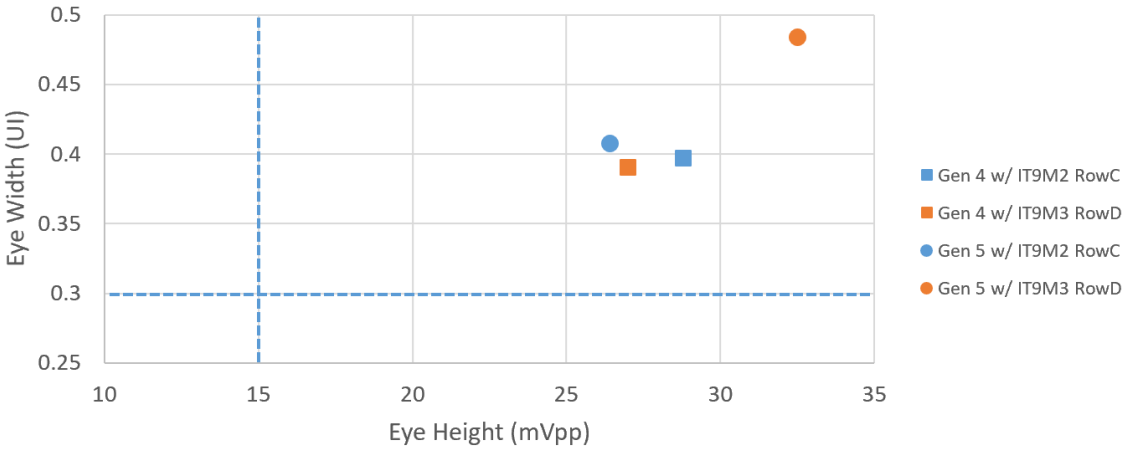


Figure 4-38 Plot showing Eye results relative to specification limits

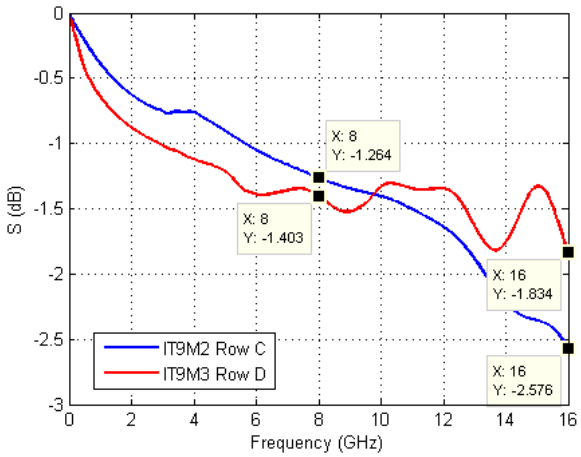


Figure 4-39 Comparison of Connector-only performance between IT9M2 Row C and IT9M3 Row D

4.4 Propagation Delay

4.4.1 Propagation Delay Overview

*Each blade in **IT9** has different length, shown in 4.4.2 Please be aware of the signal distance difference when designing PWB.*

4.4.2 Signal Path Length

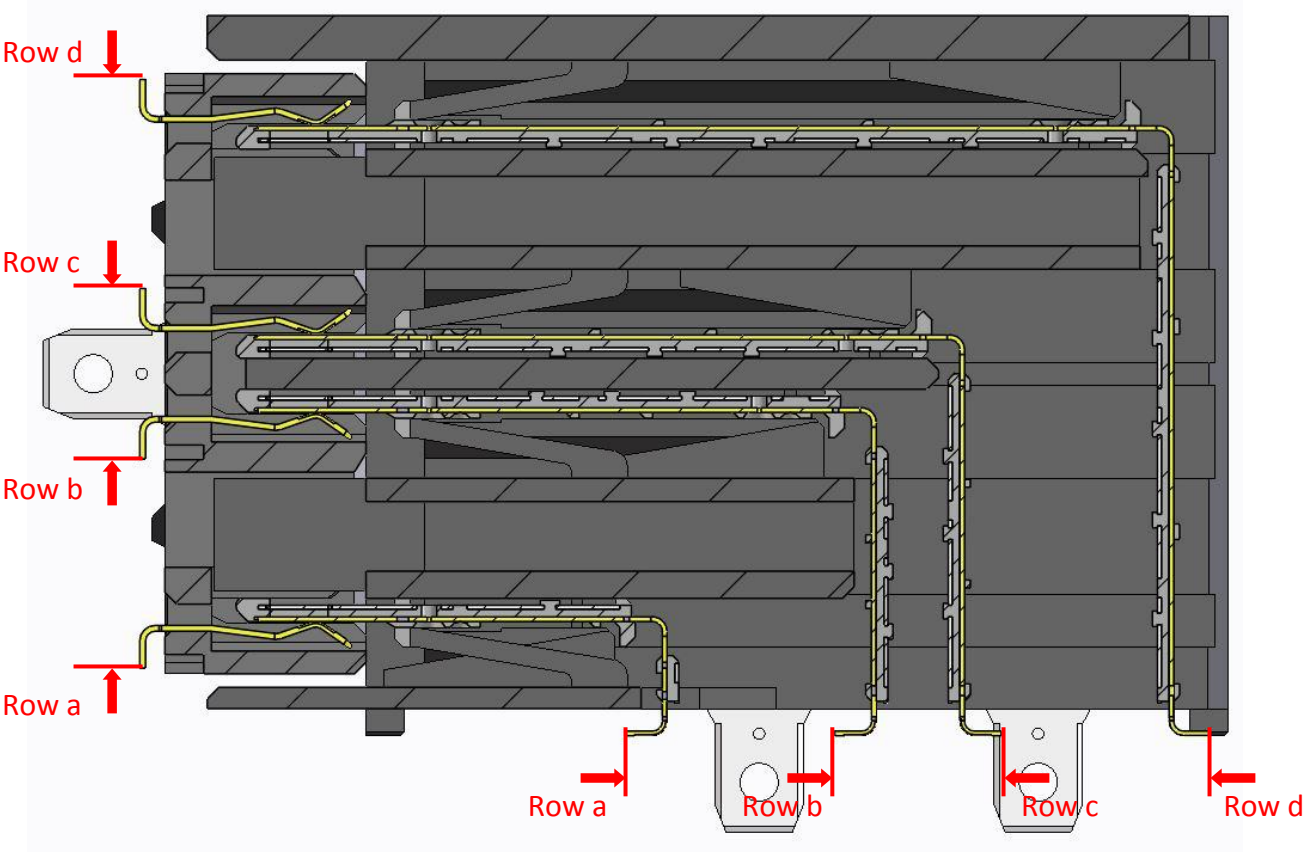


Figure 4-40 IT9 Cross Section

4.4.3 Propagation Delay for IT9

- Input Voltage : 1V
- Tr.(Input signal) : 25ps (20-80%)

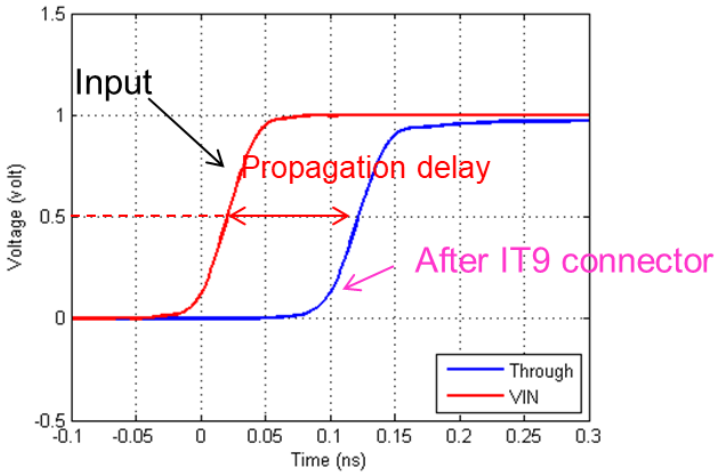


Fig4-41 Propagation Delay

<IT9M2 Series (84,224 Pos.)>

	Inner row ⟷ Outer row				Unit
	Row a	Row b	Row c	Row d	
Signal path length	17660	28460	32620	43420	µm
	695.3	1120.5	1284.3	1709.4	mils
Propagation delay - Single ended	115.6	170.85	193.49	256.56	ps
Propagation delay - Differential	110.56	164.43	186.3	249.19	ps

Table 4-2 Propagation Delay for IT9M2 Series

<IT9M3 Series (152 Pos.)>

	Inner row ⟷ Outer row				Unit
	Row a	Row b	Row c	Row d	
Signal path length	18160	28960	33120	43920	µm
	715.0	1140.16	1303.94	1729.14	mils
Propagation delay - Single ended	109.54	169.11	188.7	242.06	ps
Propagation delay - Differential	104.02	162.59	181.8	231.59	ps

Table 4-3 Propagation Delay for IT9M3 Series

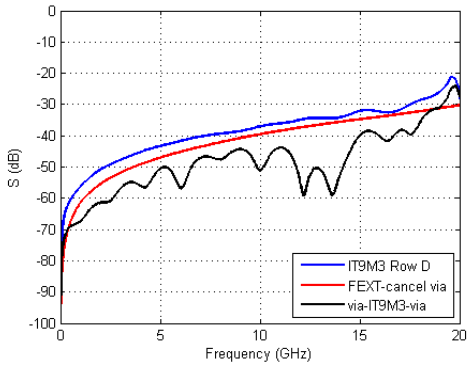
4.5 Signal Integrity for FEXT Cancellation Via

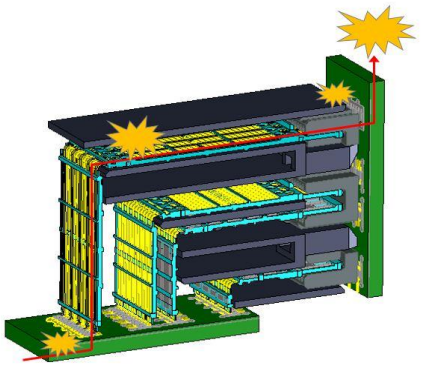
FEXT cancellation via, ***patented by Hirose (patent No. US9,554,455),*** *is recommended to be implemented when designing PWBs for* ***IT9****.* ***This design is only permitted to be used for IT9, or any other Hirose products.***
Example of FEXT cancel via design is shown in section 5.5 Via design, Routing Example.

(Basic method for FEXT cancellation)

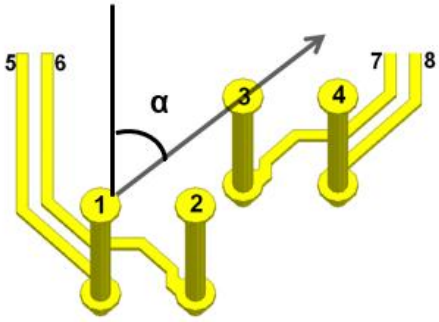
Reduce total differential FEXT of connector + vias to less than the FEXT of connector itself

- *Manipulate single-ended terms to achieve desired polarity for cancellation*
- Applicable to all components (e.g., package + via) in a channel





<Ex. Board-side coupled vias with offset>
Offset via allows the magnitude control.



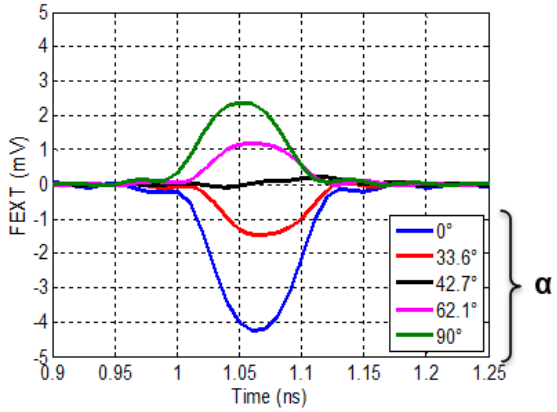


Fig4-42 FEXT in time domain

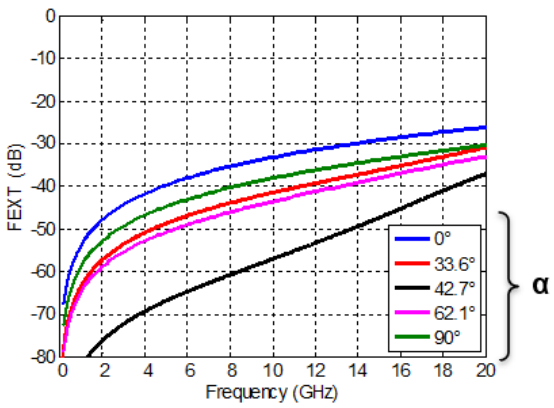


Fig4-43 FEXT in frequency domain

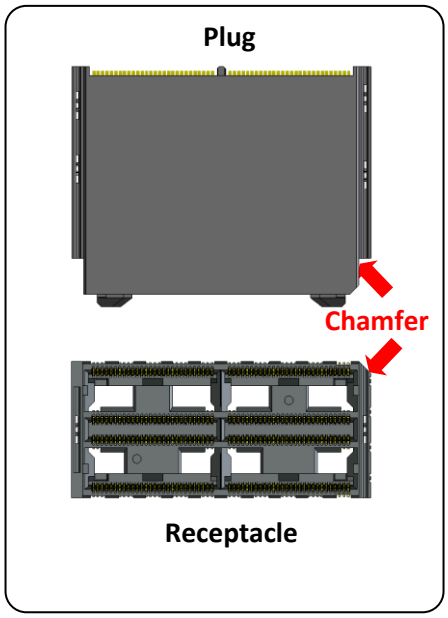
Section 5 PWB Design Information

This section discusses footprint, multi-connector systems, PWB fixing, clearance between connectors, and alignment tolerances.

5.1 Footprint

5.1.1 Polarity

Plugs and receptacle have polarization features. The chamfer direction should be matched as shown in the figure shown below; otherwise housing may deform or break and cause a system error.



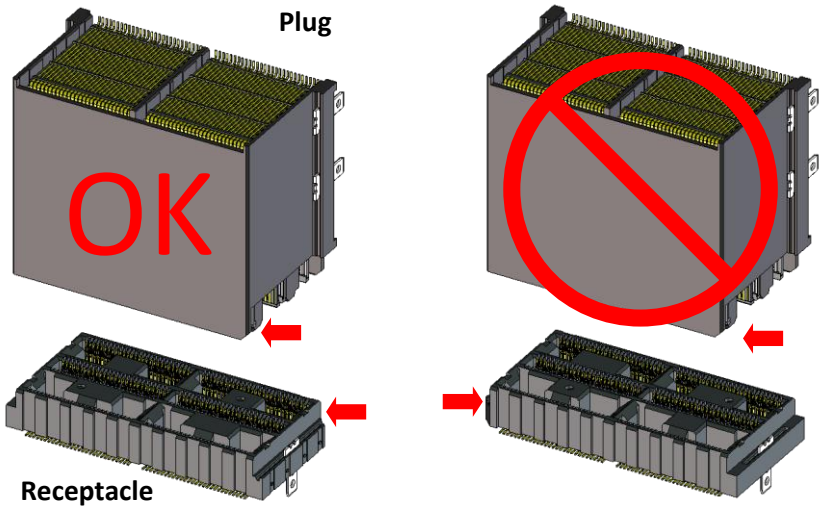


Figure 5-1 Polarization

5.1.2 Pad Specifications

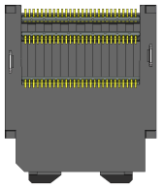
- *Pad finish: OSP (Organic Solderability Preservative) or HASL (Hot Air Solder Leveler).*

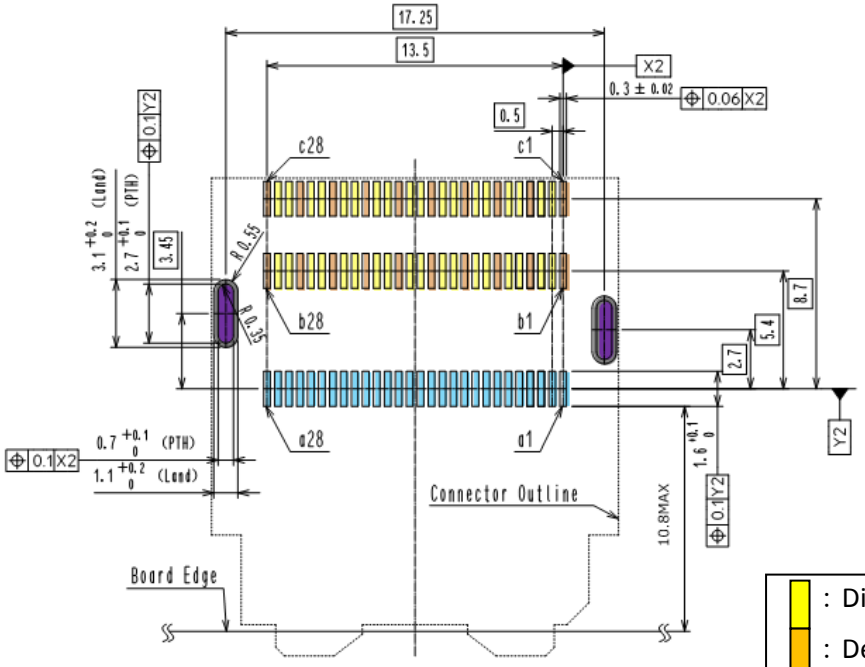
PWB pad finish is typically Organic Solderability Preservative (OSP) or Hot Air Solder Level (HASL), but the component can also be used with Electroless Nickel-Immersion Gold (ENIG), Immersion Silver, and Immersion Tin.

5.1.3 Component Footprint and Contact Assignment

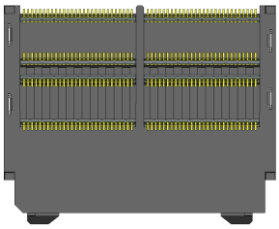
Plug

***ex. IT9M2-84P-0.5SH3* (**)**





***ex. IT9M2-224P-0.5SH4* (**)**



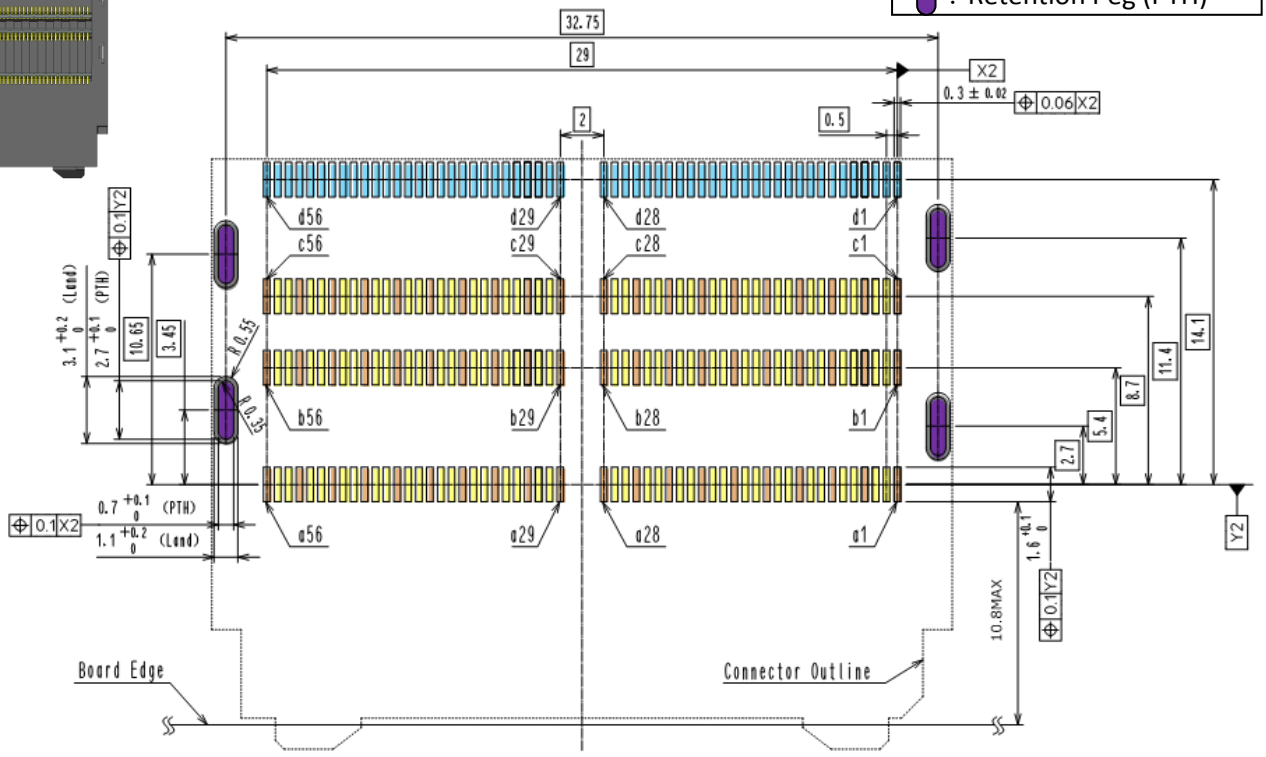
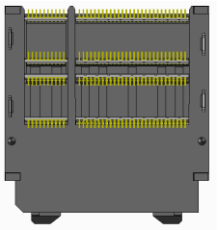


Figure 5-2a Plug Footprint (dimensions in mm)

Plug

ex. IT9M3-152P-0.5SH4 (**)



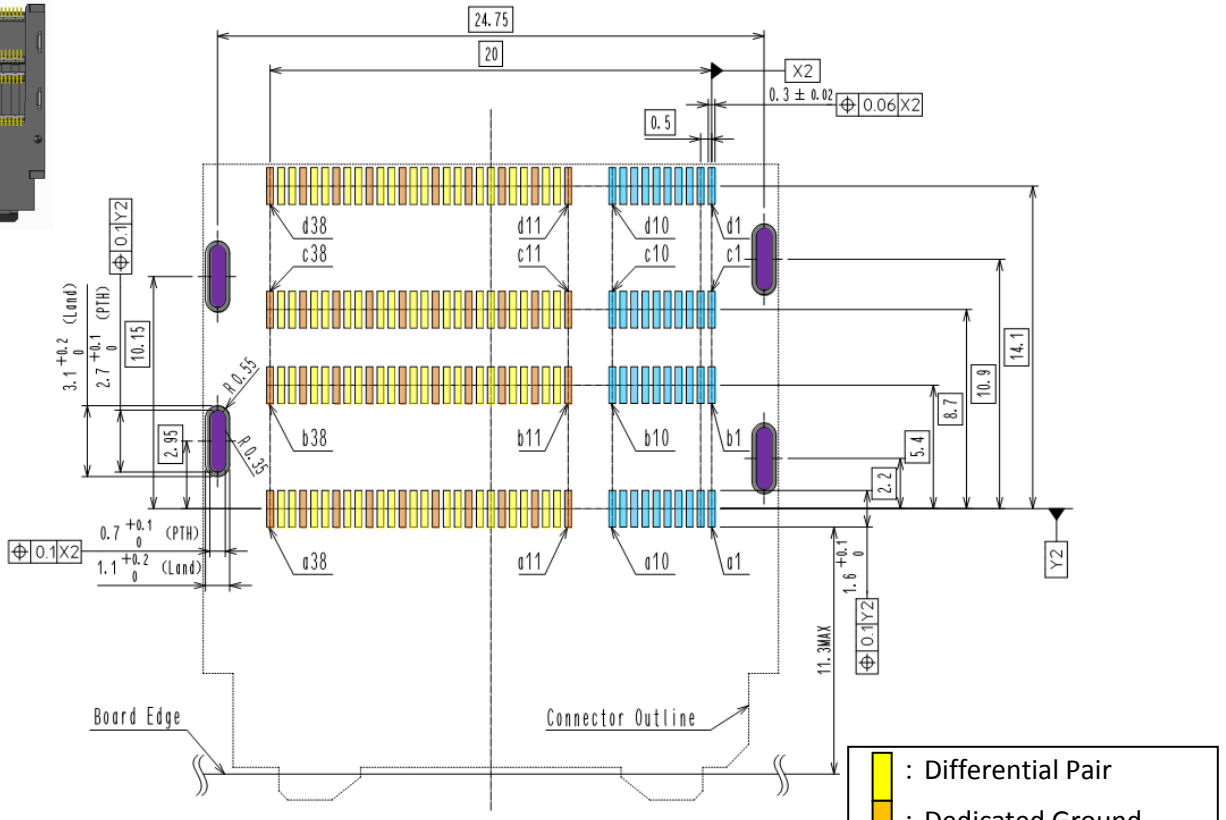
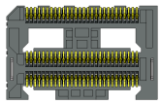


Figure 5-2b Plug Footprint (dimensions in mm)

Receptacle

ex. IT9M2-84S-0.5SV3 (**)



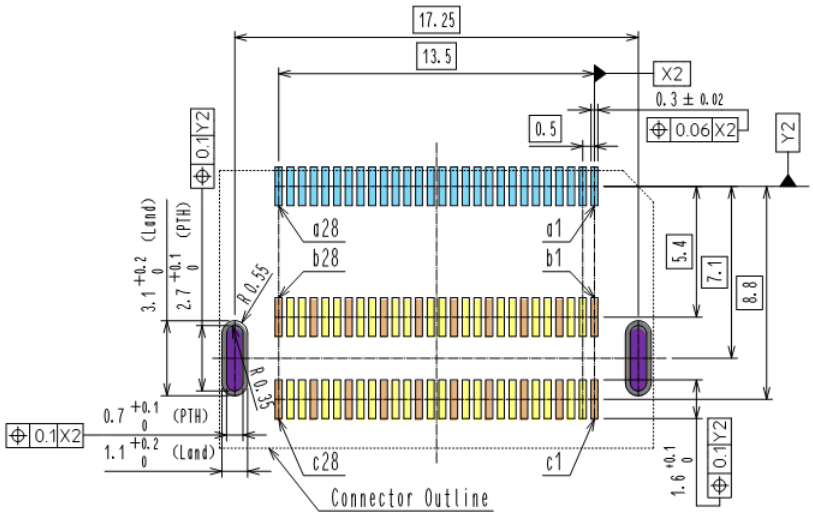
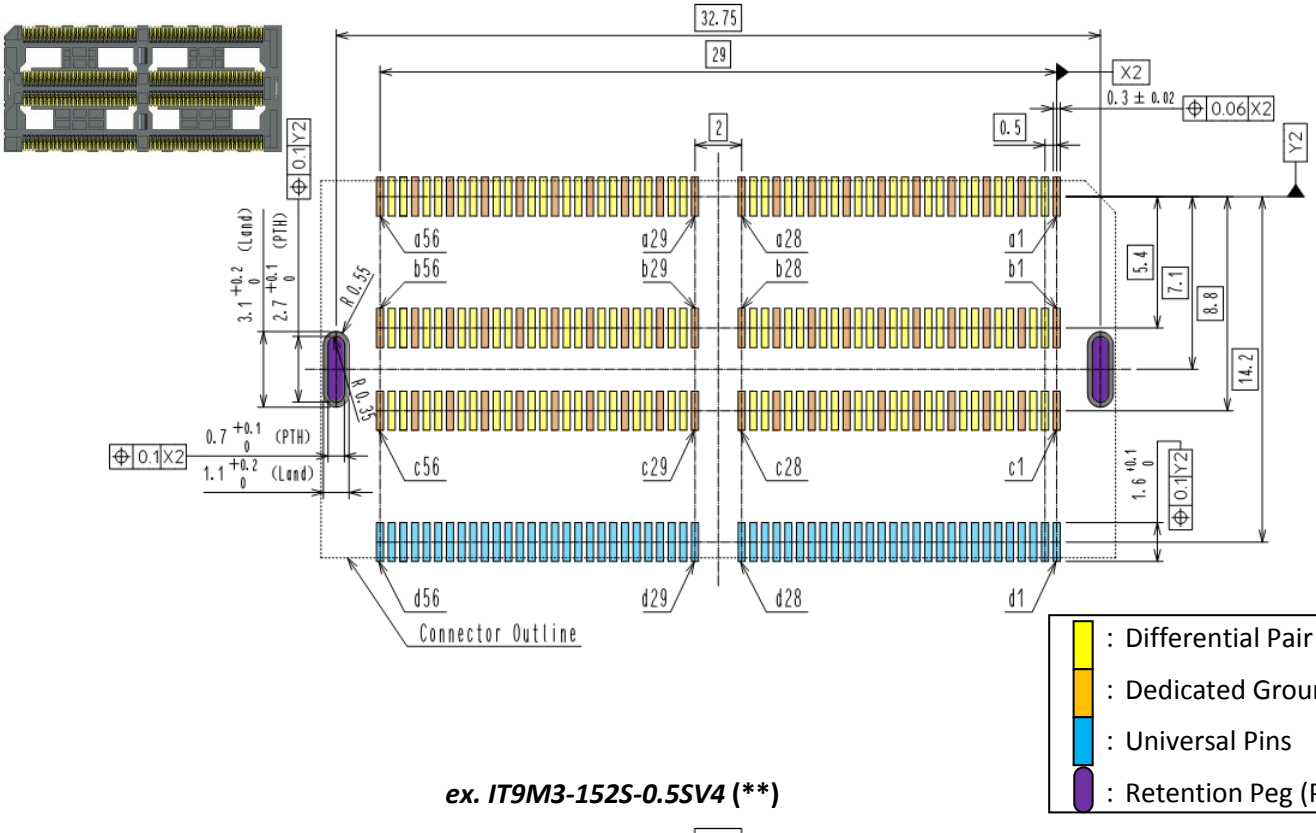


Figure 5-3a Receptacle Footprint (dimensions in mm)

Receptacle

ex. IT9M2-224S-0.5SV4 (**)



ex. IT9M3-152S-0.5SV4 (**)

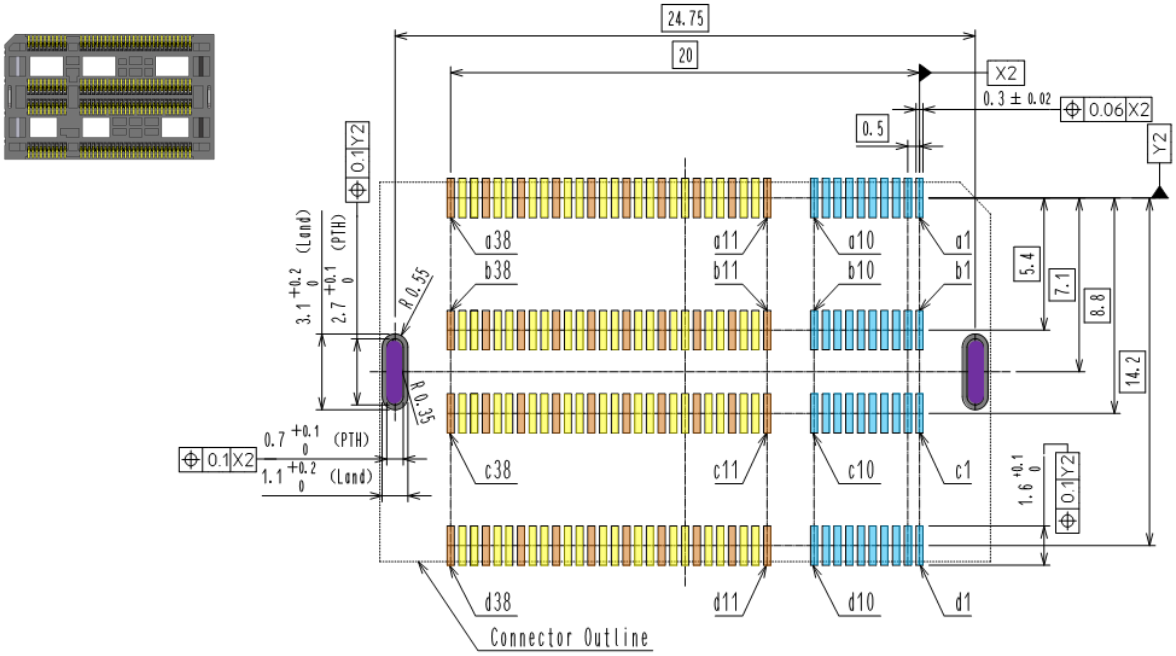


Figure 5-3b Receptacle Footprint (dimensions in mm)

5.2 Multi-Connector Systems

*The **IT9** Series connectors can be used alone or in combination with compatible connectors.*

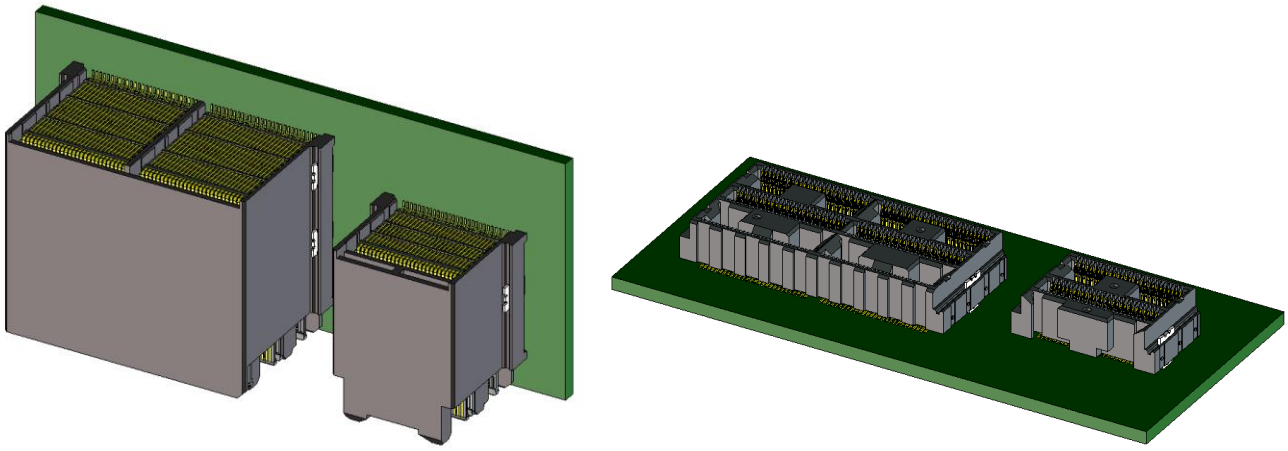


Figure 5-5 Combination Use

Please note that combination use may cause high mating/un-mating force, or mating imbalance.

5.3 PWB Fixing

PWB's are necessary to be fixed with each other to protect the SMT solder joints and connectors.

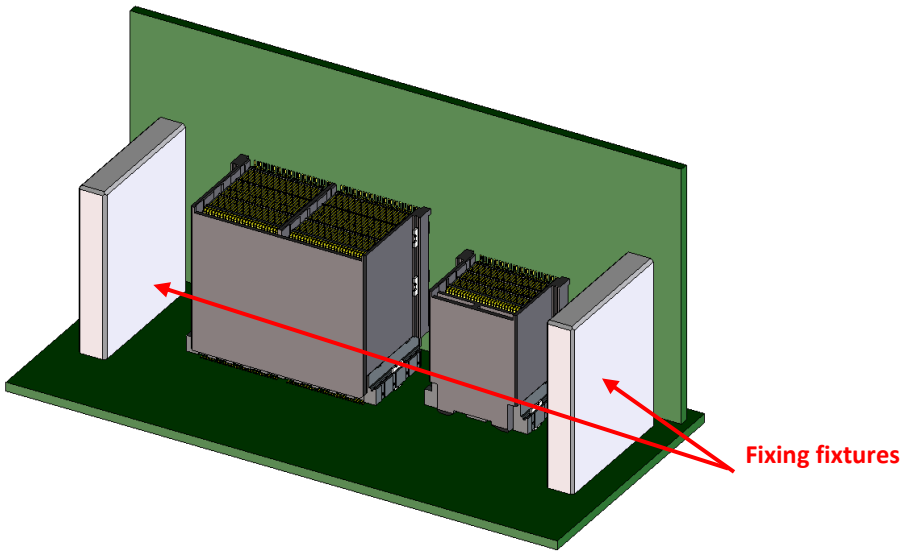


Figure 5-6 PWB Fixing

5.3.1 PWB Fixing Location

PWB's are recommended to be fixed nearby the connectors.

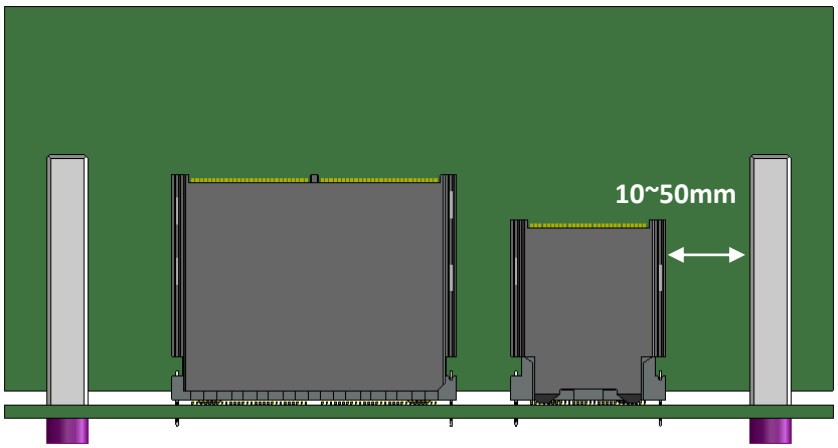


Figure 5-7 Fixing Equipment

Fixing fixtures should be located 10 - 50 mm from the corners of the plugs or receptacles to prevent excessive mechanical loading on the interconnections.
If assembly will be subjected to vibration, fixtures should be designed and located to prevent resonance.

5.4 Clearance between Connectors and Other Components/PCB Edge

5.4.1 Clearance between Connectors and Other Components

*The **IT9** series connectors keep-out area is required for re-work capability. This allows around the connector housing for re-work tooling and nozzles.*

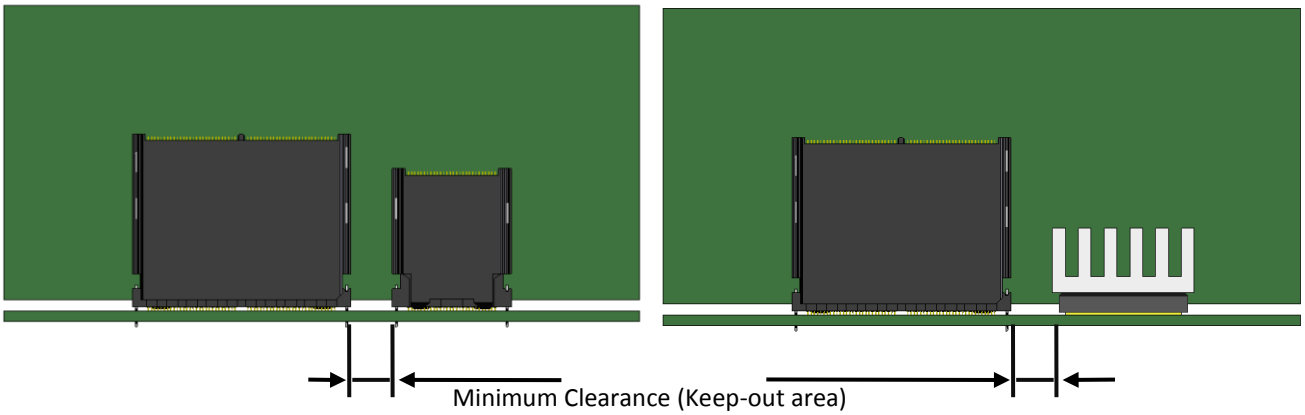


Figure 5-8 Clearance

Sensitive device means ; Leaded Fine Pitch, BGA/CGA, etc.
Common device means ; Leaded 1.27mm Pitch, Chips, etc.

5.4.2 Clearance between the Connector and PWB Edge

Please communicate with the CEM regarding the clearance, especially when requiring the top side reflow.

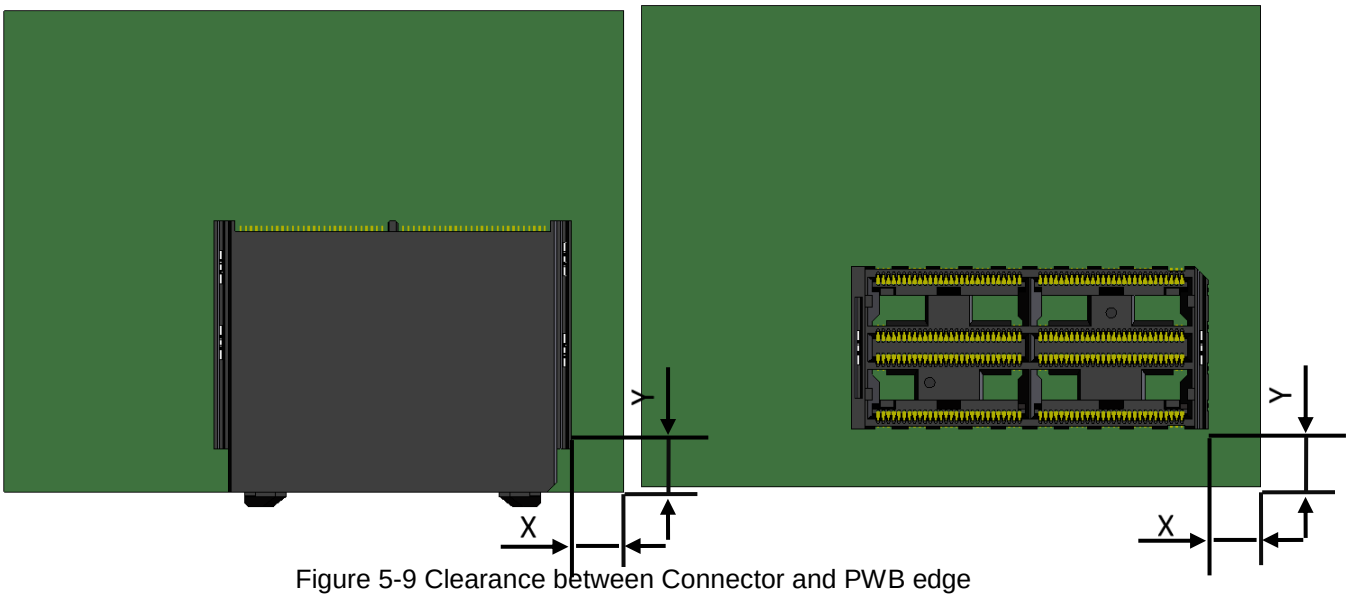


Figure 5-9 Clearance between Connector and PWB edge

5.5 Via design, Routing Example

Since IT9 is the four rows surface mount connector, traces can be routed on the surface layer directly out of the connector footprint. Differential pairs can be routed differentially with some coupling between the traces, as shown in Figure 5-10. And this via design is one of example for FEXT cancellation via.

**If need the via optimization for a specific stack-up, please contact to Hirose.*

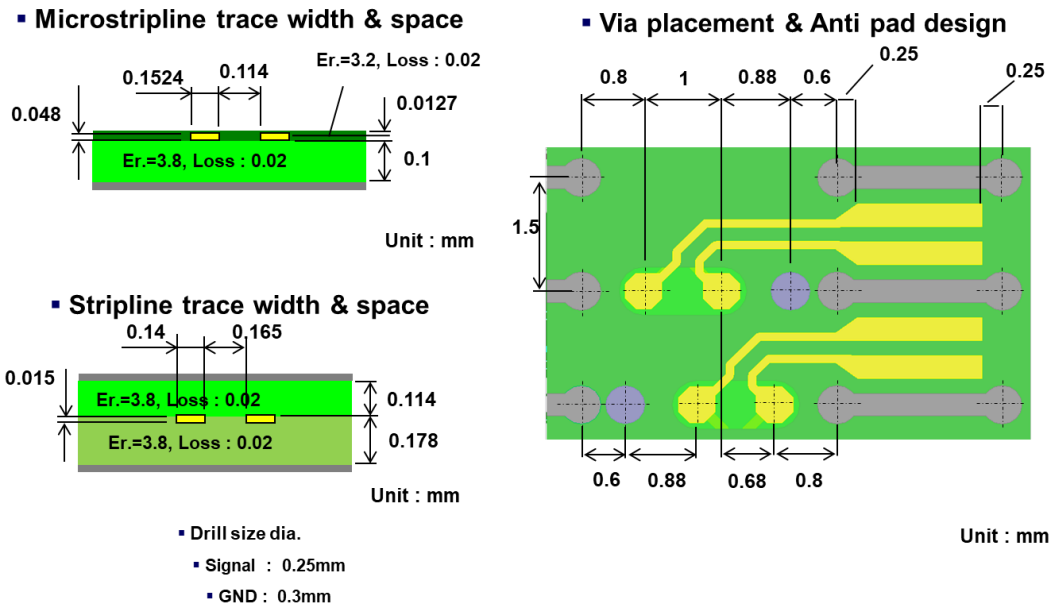


Figure 5-10 Example for FEXT cancel via and routing differential traces from the IT9 footprint

For inner layer routing, Figure 5-11 shows an example routing scheme for high speed differential pairs. Note IT9 series 3 row type will require 3 separate routing layers, 4 row type will require 4 separate routing layers to use.

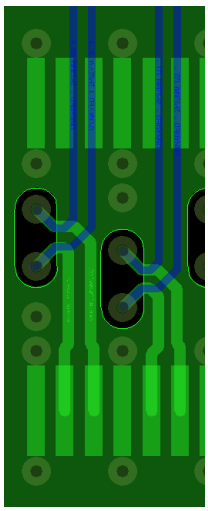


Figure 5-11 Example of routing on inner layers underneath IT9 connector

Section 6 Stencil Printing Information

This section discusses stencil printing.

6.1 Solder Paste Selection

*The **IT9** connectors are compatible with lead-free solder pastes. The user should assure that the solder alloy used in the assembly process is compatible with the appropriate component configuration.*

ex.

Manufacturers: Senjyu Metal Industry Co., Ltd

Product Part No. : M705-GRN360-K2-V

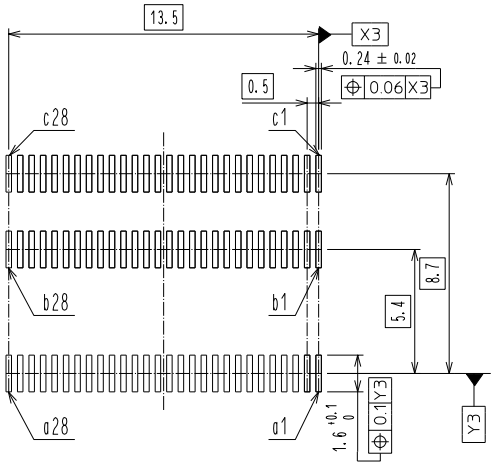
Alloy Composition (wt%): Sn-3.0Ag-0.5Cu

6.2 Recommended Stencil Designs

Recommendations for the stencil thickness is 0.13mm. Stencil aperture size and/or thickness may need to be adjusted according to circumstances of each assembly line.

Plug

***ex. IT9M2-84P-0.5SH3* (**)**



***ex. IT9M2-224P-0.5SH4* (**)**

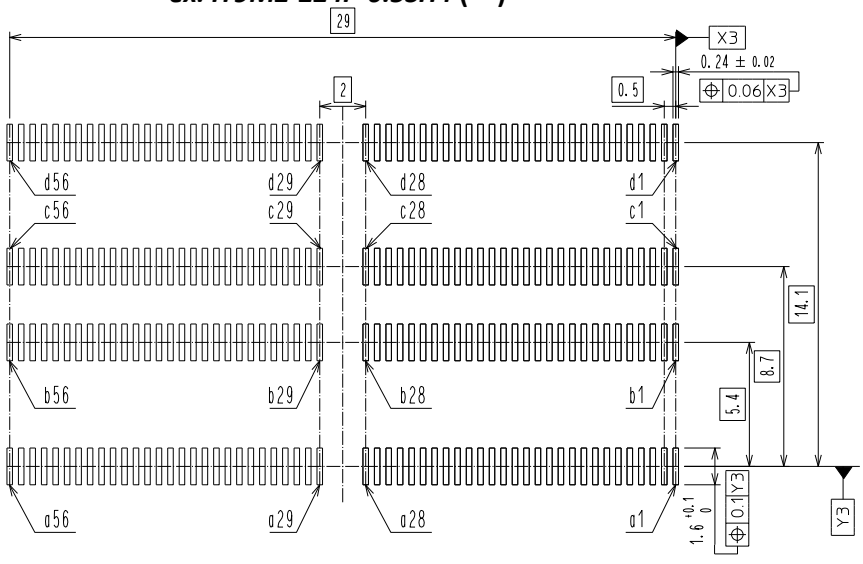


Figure 6-1a Plug Stencil Patterns (dimensions in mm)

Plug

***ex. IT9M3-152P-0.5SH4* (**)**

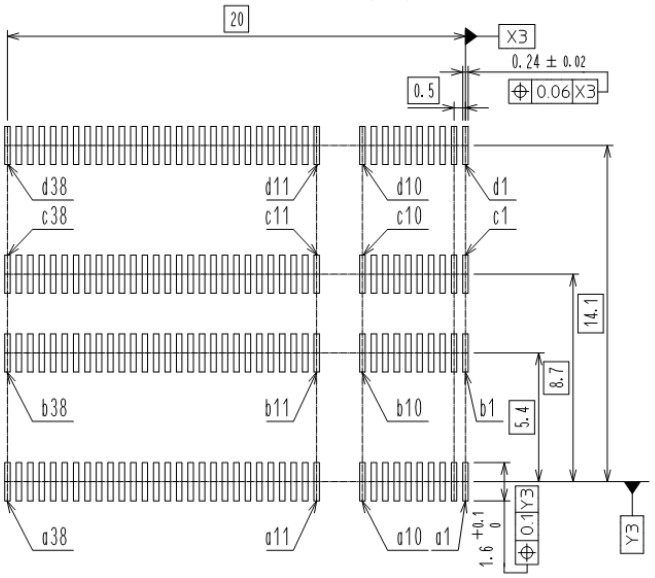
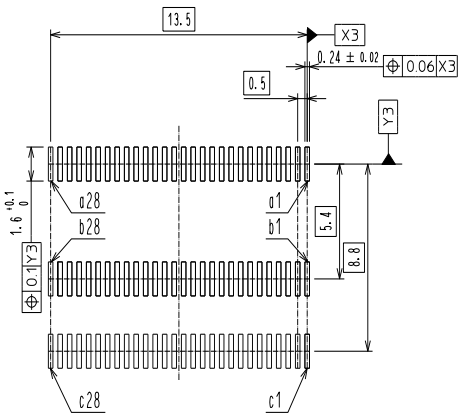


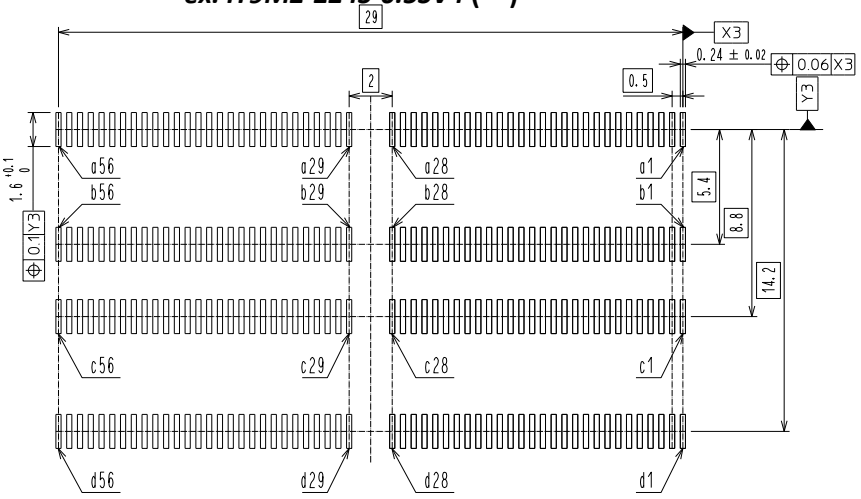
Figure 6-1b Plug Stencil Patterns (dimensions in mm)

Receptacle

***ex. IT9M2-84S-0.5SV3* (**)**



***ex. IT9M2-224S-0.5SV4* (**)**



***ex. IT9M3-152S-0.5SV4* (**)**

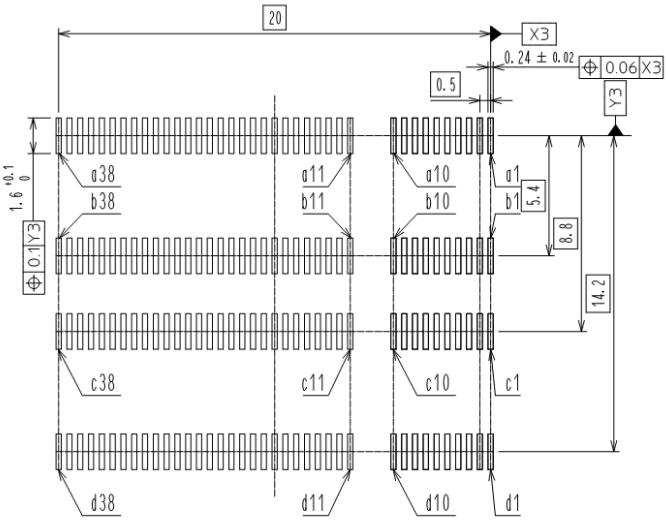


Figure 6-2 Receptacle Stencil Patterns (dimensions in mm)

Please refer to individual product drawings for details.

Section 7 Pick and Place Information

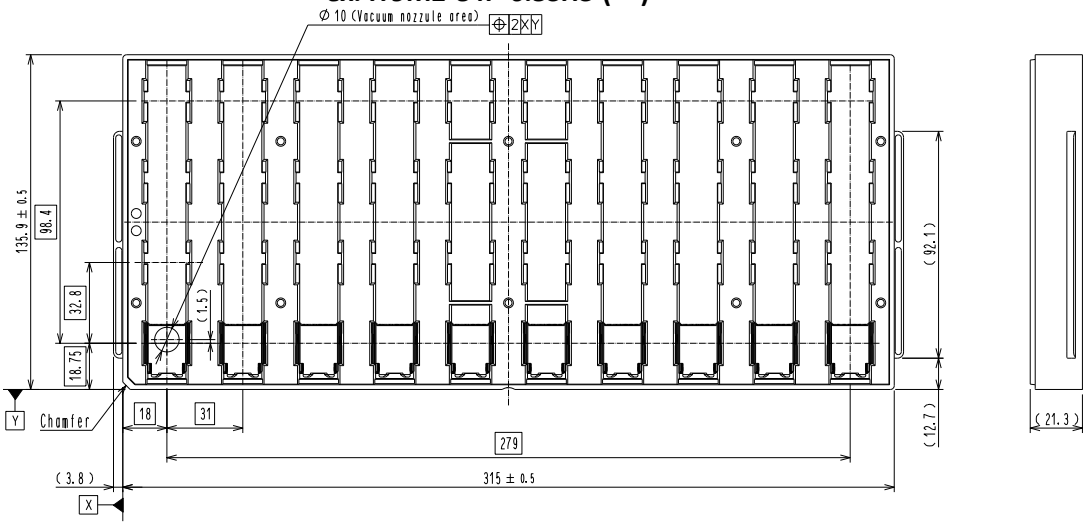
This section discusses connector pick and place.

7.1 Packaging

7.1.1 Plug

IT9 *plug components are shipped in JEDEC hard trays as shown below.*

***ex. IT9M2-84P-0.5SH3* (**)**



***ex. IT9M2-224P-0.5SH4* (**)**

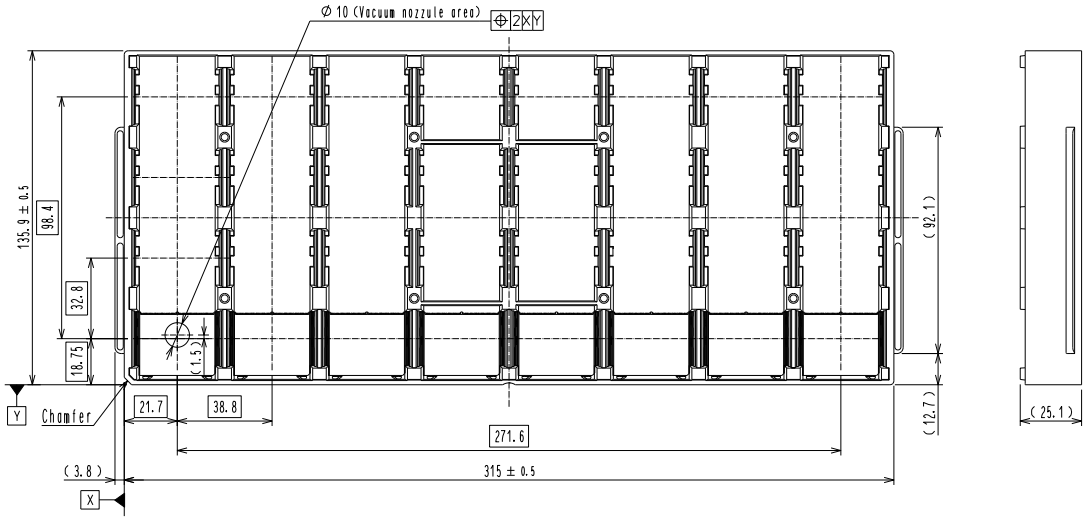


Figure 7-1a Hard Tray for IT9 Plug (dimensions in mm)

***ex. IT9M3-152P-0.5SH4* (**)**

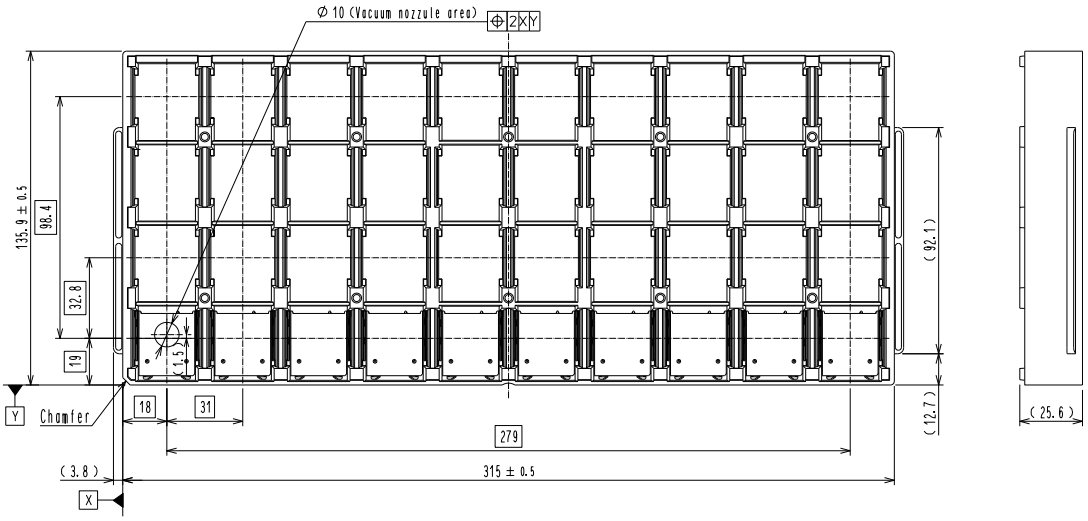


Figure 7-1b Hard Tray for IT9 Plug (dimensions in mm)

Please refer to individual product drawings for details.

7.1.2 Receptacle

IT9 *receptacle components are shipped in embossed carrier tape with pick and place adhesive tapes attached on as shown below.*

***ex. IT9M2-84P-0.5SH3* (**)**

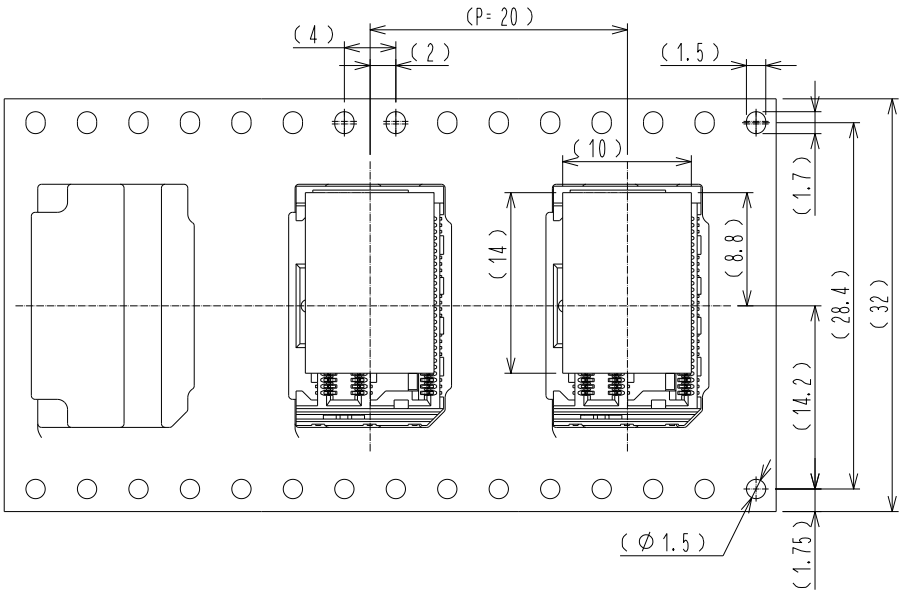
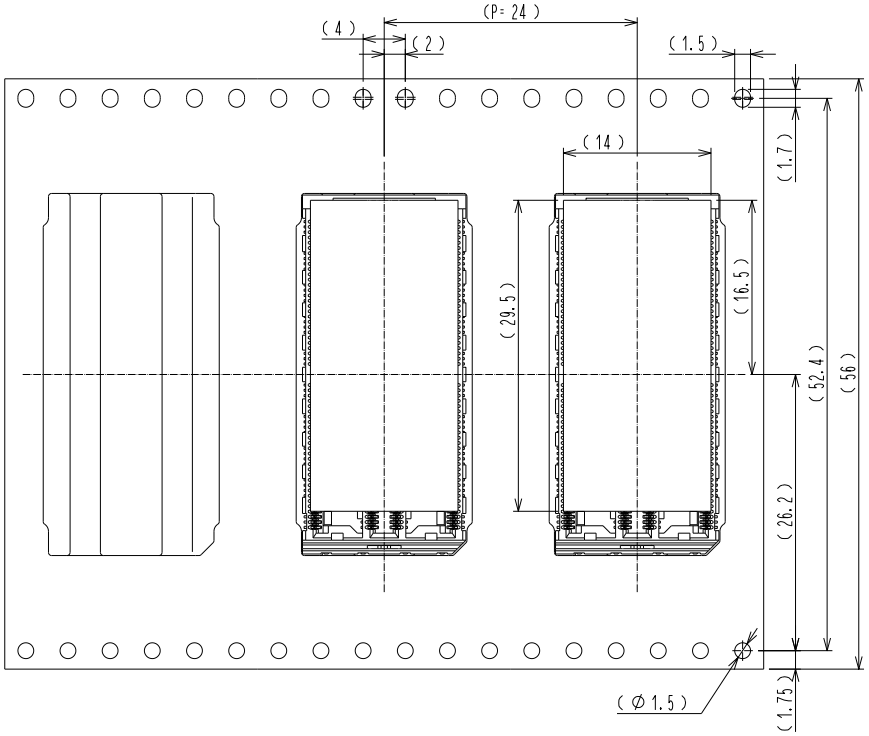


Figure 7-2a Embossed Carrier Tape for IT9 Receptacle (dimensions in mm)

***ex. IT9M2-224P-0.5SH4* (**)**



***ex. IT9M3-152P-0.5SH4* (**)**

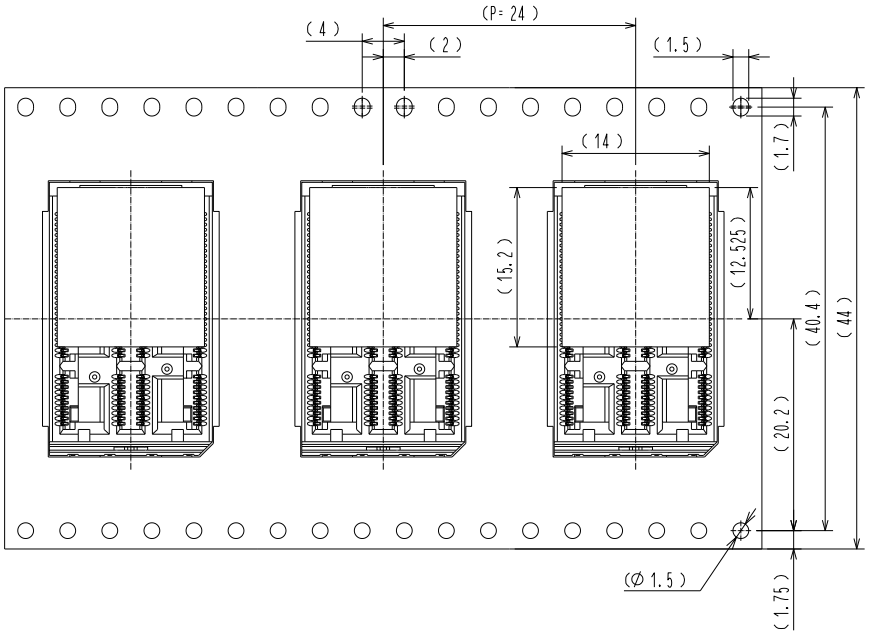


Figure 7-2b Embossed Carrier Tape for IT9 Receptacle (dimensions in mm)

Please refer to individual product drawings for details.

7.2 Pre-bake

*The connector body materials do not absorb water from the atmosphere; therefore pre-bake is not required for **IT9** receptacles and plugs.*

7.3 Pick Point

*Pick locations and dimensions for **IT9** connectors are shown below. Pick points are located at the approximately geometric centers of connectors.*

***ex. IT9M2-84P-0.5SH3* (**)** ***ex. IT9M2-224P-0.5SH4* (**)** ***ex. IT9M3-152P-0.5SH4* (**)**

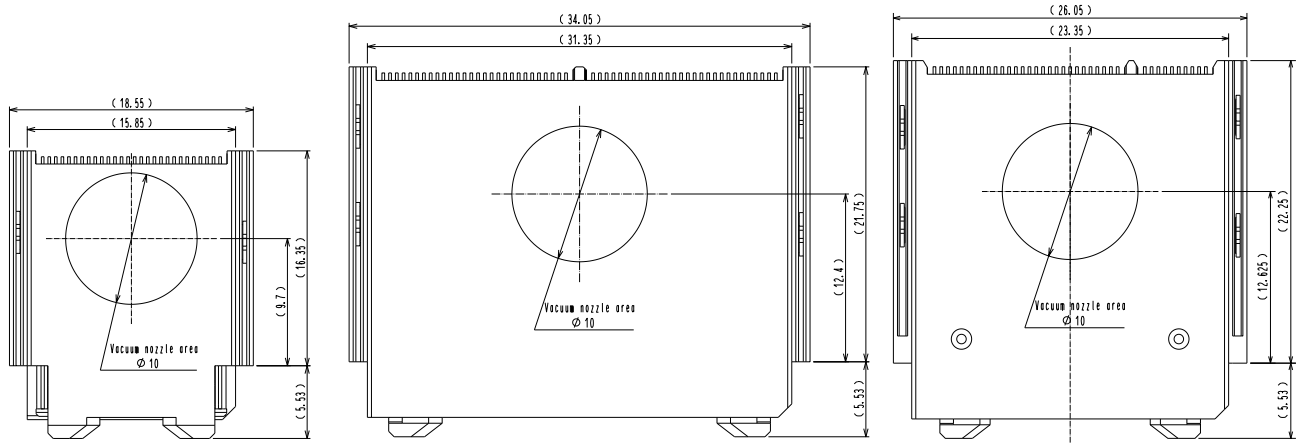


Figure 7-3 Pick Points of IT9 Plug (dimensions in mm)

***IT9** receptacles have adhesive tapes for vacuum pick up.*

***ex. IT9M2-84S-0.5SV3* (**)** ***ex. IT9M2-224S-0.5SV4* (**)** ***ex. IT9M3-152S-0.5SV4* (**)**

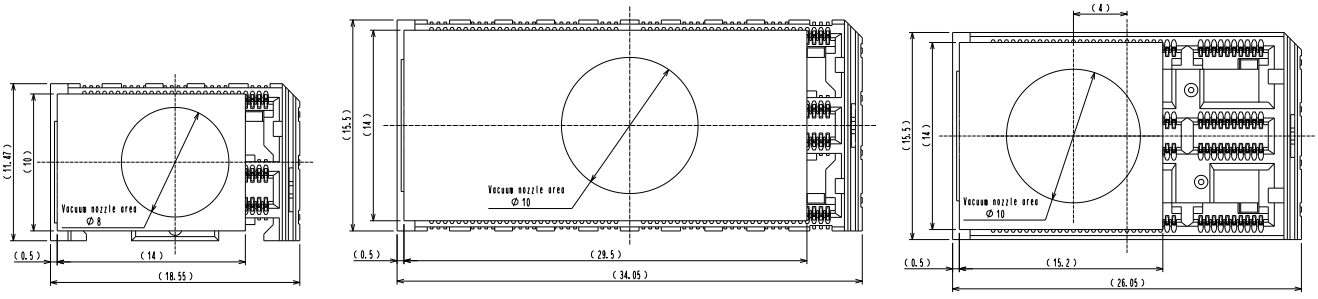


Figure 7-4 Pick Points of IT9 Receptacle (dimensions in mm)

Please refer to individual product drawings for details.

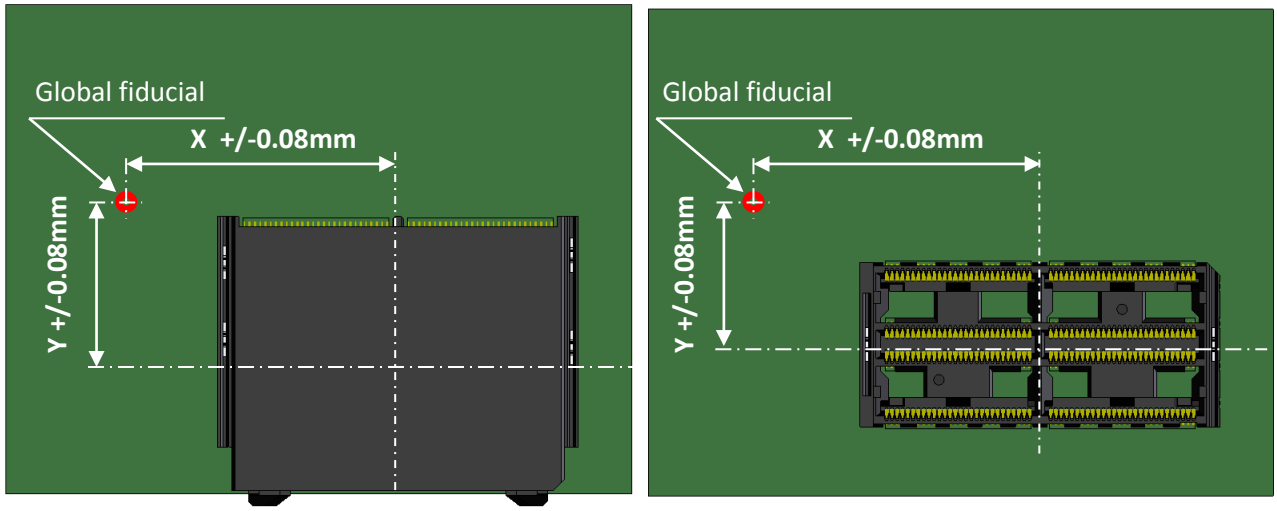
7.4 Polarity

***IT9** connectors have polarity as mentioned on Chapter 5.1.1.*

7.5 Mounting Tolerances

Mounting tolerances of ± 0.08mm are required for robust SMT assembly and to ensure proper mating fit in case of multiple connector use:

***ex. IT9M2-224P-0.5SH4* (**)** ***ex. IT9M2-224S-0.5SV4* (**)**



Plug Receptacle

Figure 7-5 Mounting Tolerance

Section 8 Reflow and Solder Bath Processing Information

*This section discusses **IT9** reflow and solder bath processing.*

8.1 Reflow Profile for Lead-free Solder

Profile Feature	Condition	Note
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150 °C 200 °C 60-120 seconds	Soak requirements should be determined by board design, oven capability, and paste activation requirements. Caution- "oversoaking" may exhaust flux and affect soldering.
Ramp-up rate (TL to Tp)	3 °C/second max.	Other components may limit ramp rate to 2°C/sec.
Liquidous temperature (TL) Time (tL) maintained above TL	217 °C 60-150 seconds	Shorter t_L may require higher peak temperature.
Peak package body temperature (Tp)	245 °C max.	Cooler peak temperatures may require longer t_L. For users Tp must not exceed the classification temp (T_C) of 250°C.
Time (tp)* within 5 °C of the specified classification temperature (Tc)	30 seconds max.	
Ramp-down rate (Tp to TL)	6 °C/second max.	
Package body exposure limit at maximum temperature	5 seconds	Adjust profile if maximum exposure limits are approached or exceeded.

All temperatures refer to the center of the connector body, measured on the connector body surface that is facing up during assembly reflow. Reflow profiles in this document are based according to IPC/JEDEC J-STD-020D.1 and are for preconditioning. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in the table above.

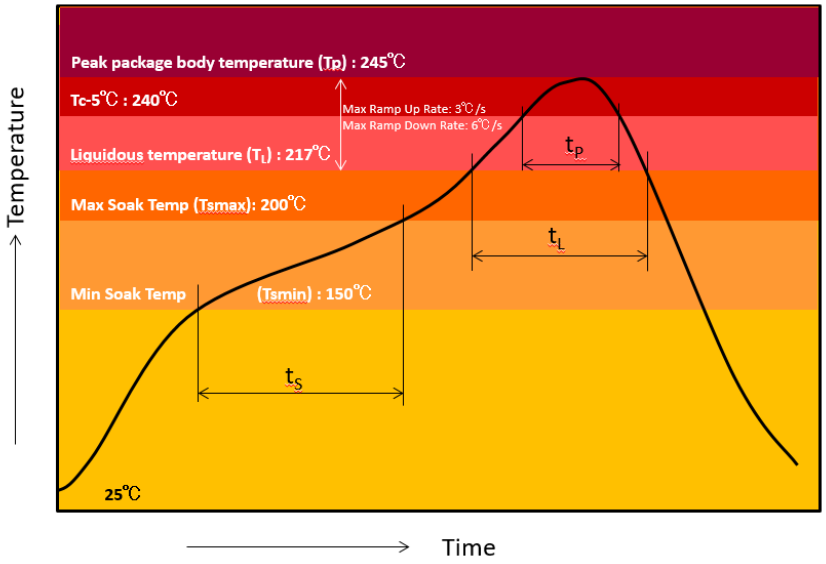


Figure 8-1 Thermal Profile Ranges

Different solder pastes have different thermal performance characteristics. Consult with paste manufacturer for optimum profile settings.

8.2 Other Important Factors

Check thermal exposure limits of PWB laminate.

8.3 Nitrogen Environment

The use of nitrogen to inert the reflow process can:

1. *Improve solder wetting by limiting oxidation on metal surfaces*
2. *Allow lower peak temperatures and/or lower times above liquidus*
3. *Improve the cleanability of flux residues*

The benefits of using nitrogen increase as oxygen levels are decreased; optimum oxygen levels must be 1500 ppm or less determined by the assembler.

*Generally speaking, nitrogen inerting opens the reflow window for most electronic components. The use of nitrogen in the reflow process will likely improve the soldering performance of the **IT9** connector.*

8.4 Solder Bath Information

*Solder bath can be used for **IT9** retention peg soldering.*

8.4.1 Solder Selection

*The **IT9** connectors are compatible with lead-free solder. The user should assure that the solder alloy used in the assembly process is compatible with the appropriate component configuration.*

ex.

Manufacturers: Senjyu Metal Industry Co., Ltd

Product Part No. : M705

Alloy Composition (wt%): Sn-3.0Ag-0.5Cu

8.4.2 Recommended Soldering Condition

Profile Feature	Condition
Temperature of solder bath	260±5℃
Immersion duration	10±1 seconds

8.4.3 Recommended Rework Condition

Please refer to Figure 8-1 for recommended thermal profile for rework. The user should not reuse the connector once it is removed from the PWB. If the PWB is properly cleaned after removal, then the PWB is appropriate for reuse.

Section 9 Assembly Process Information

*This section of the Design Note discusses the summarized **IT9** assembly process.*

9.1 Mating Self Alignment

***IT9** Series can accept mating self-alignment of up to ±1.6mm tolerance in the X-axis and up to ±1.6mm in the Y-axis.*

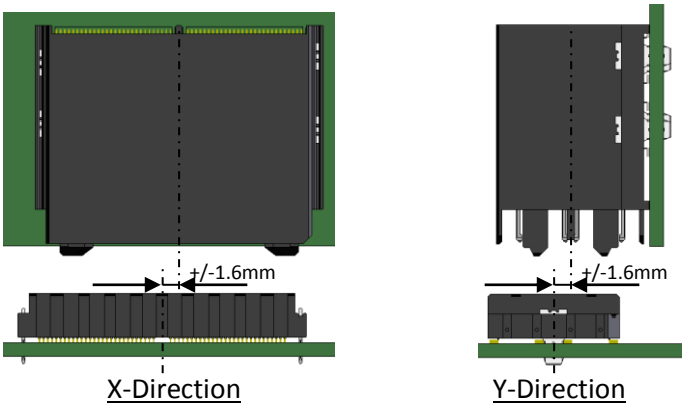


Figure 9-1 Self Alignment

These values do not include the influence of misalignment in other axes nor the rotation/inclination in the same time, except for the misalignment in the single axis shown in each figure.

9.2 Mated State Tolerances

***IT9** Series can accept mating tolerances of up to ±0.16mm tolerance in the X-axis and up to ±0.16mm in the Y-axis.*

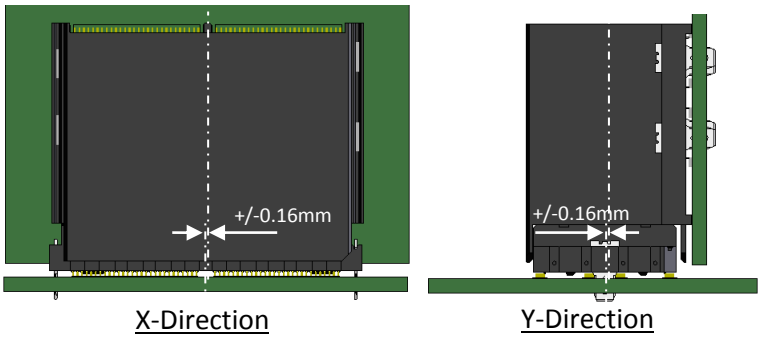


Figure 9-2 Mating Tolerances

These values do not include the influence of misalignment in other axes nor the rotation/inclination in the same time, except for the misalignment in the single axis shown in each figure.

This structure is not for vibration absorption. Sufficient fixing fixtures (mentioned in Chapter 5.3) are necessary to support the PWBs and protect the SMT solder joints and connectors.

9.3 Wiping Length

IT9M2 *Series contact wiping length is 2 mm (NOM).*
IT9M3 *Series contact wiping length is 1.5 mm (NOM).*

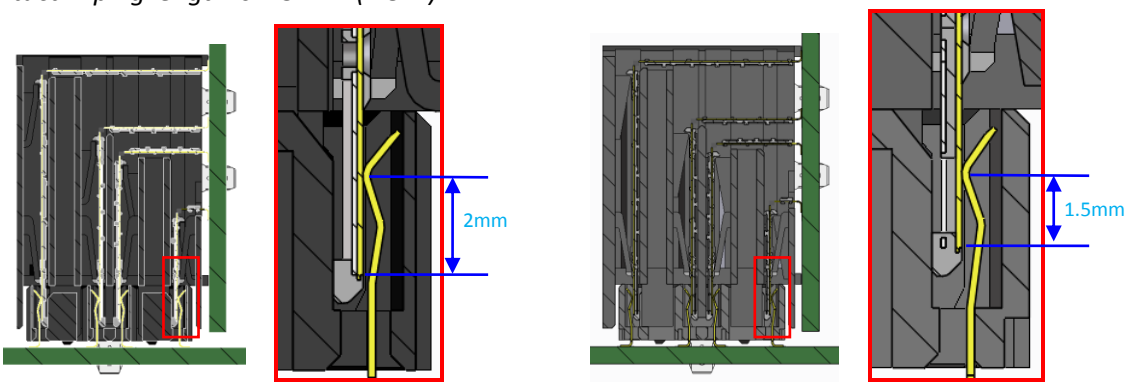


Figure 9-3 Wiping Length

9.4 Overall Assembly and Disassembly Process

In mating and un-mating operation, 0° for following angles are preferred. In the case that keeping 0° is difficult, the following maximum angles should not be exceeded during manual installation and the removal of the daughter card (shown below)

- *Longitudinal: 2.5°*
- *Lateral: 2.5°*

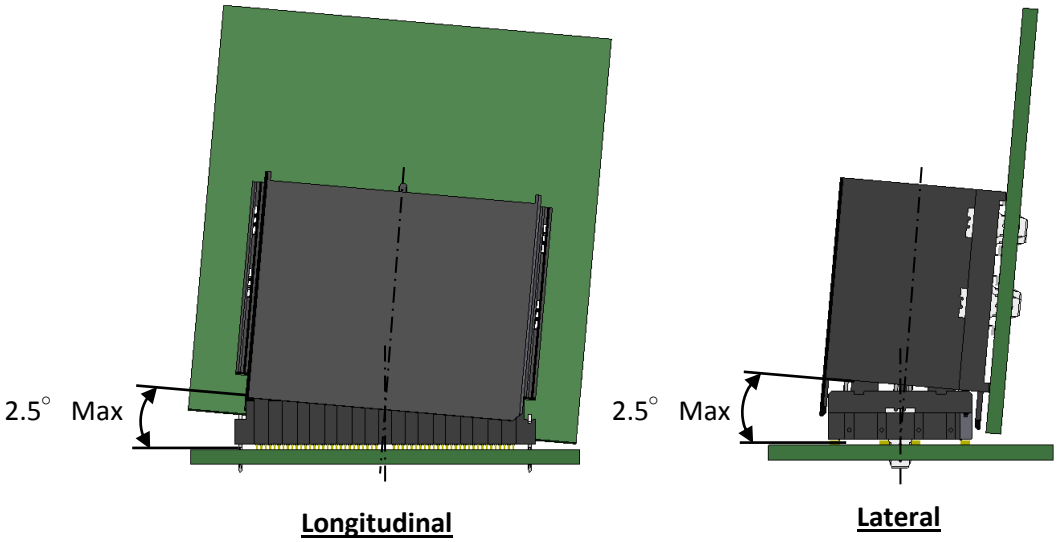


Figure 9-4 Angles during Manual Installation

Please consider to keep allowable angles (Figure 9-4) and the orientation of the daughter card for manual assembly during the design process. These values do not include the influence of misalignment in other axes nor the rotation/inclination in the same time, except for the misalignment in the single axis shown in each figure. Hirose also strongly recommends the use of fixing fixtures as mentioned on Chapter 5.3.

Section 10 Technical Document Library

Following data and documents are available.

10.1 Technical Data

No	Item	Format	File name (Ex.)
1	Simplified 3D model	STEP / IGES	TBD
2	Touchstone model	Touchstone	TBD
3	Allegro foot print	DRA	TBD

10.2 Technical Document

No	Item	Format	File name (Ex.) or Document number
1	2D drawing	PDF	EDC-364817 EDC-364818 EDC-379970 EDC-369004 EDC-369005 EDC-379971
2	Spec sheets	PDF	ELC-364817 ELC-364818 ELC-379970 ELC-369004 ELC-369005 ELC-379971
3	Quality evaluation test report	PDF	TR0636E-10396
4	Vibration and shock test report	PDF	TR0636E-10397
5	Packaging reliability test report	PDF	TR0636E-20403
6	Temperature rise report	PDF	TR0636E-20425
7	Soldearability evaluation test report	PDF	TR0636E-20432
8	Design notes	PDF	ETAD-F0842
9	PCB Routing Guideline	PDF	16HSI-S038-R1-O
10			

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