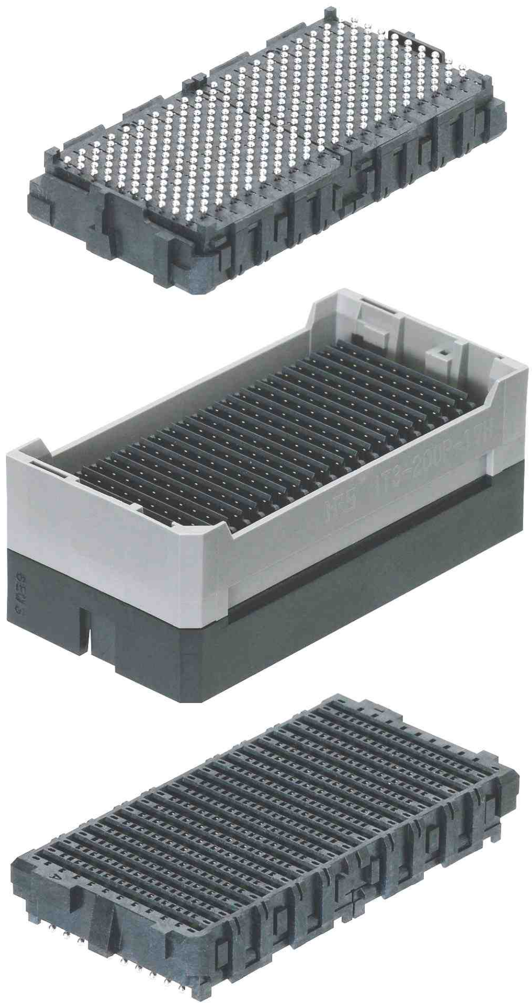
Hirose *IT3* ™

Connector System

Design Notes



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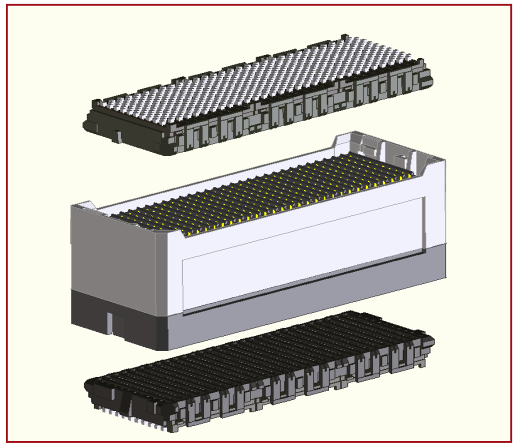
Revision No.	***Description (Major changes)***	***Date***
0.9	Preliminary release	Dec 4, 2009
0.91	Corrected footprint information and integration of some technical terms with other documents	Dec 30, 2009
0.95	Addition of manual interposer assembly and disassembly procedures	Jan 18, 2010
0.96	Update on height variation and interposer assembly cap	Jan 14, 2011
1.00	Information on plugs and an interposer removal tool	May 4, 2011

Section 1 Introduction

*The Hirose **IT3** connector system is a three-piece mezzanine connector. Process-friendly BGA receptacles are assembled onto PWBs, and separate, configurable interposers complete the connections between circuit boards. 100, 200 and 300 signal models, with tin-lead or lead-free alloys, are available.*



Hirose *IT3* connector assembly

This section of the Design Note discusses purpose, scope, and application and interpretation.

1.1 Purpose

This technical bulletin is intended to provide basic information and product features of the Hirose ***IT3*** BGA connector system. By providing this information, Hirose believes it can help its customers to speed product development, improve quality and reliability, and limit overall system costs.

1.2 Scope

This guideline provides information useful for applications using the ***IT3*** BGA connector system. It provides information pertaining to:

a) General Information
b) Operating Characteristics
c) Signal Integrity
d) PWB design Information
e) Assembly process

This document will be updated by Hirose as required to reflect current technologies and manufacturing capabilities.

1.3 Application and Interpretation

This technical bulletin is intended to offer only general guidance and design concepts to customers. It does not limit customer designs nor guarantee results under all situations. Development of actual designs is the responsibility of each customer. Customers should consult with Hirose regarding their specific application, when, or if, any questions arise relating to these guidelines. Use of this technical bulletin is at customer's sole risk. This bulletin is provided *"AS IS"* and without warranty of any kind and Hirose *EXPRESSLY DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HIROSE DOES NOT WARRANT THAT THE GUIDELINES CONTAINED IN THIS BULLETIN WILL MEET ANY CUSTOMER'S REQUIREMENTS. FURTHERMORE, HIROSE DOES NOT WARRANT OR MAKE ANY REPRESENTATIONS REGARDING THE USE OR THE RESULTS OF THE USE OF INFORMATION CONTAINED IN THIS BULLETIN IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. UNDER NO CIRCUMSTANCE SHALL HIROSE OR ITS DIRECTORS, OFFICERS, EMPLOYEES OR AGENTS BE LIABLE FOR ANY INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES (INCLUDING DAMAGES FOR LOSS OF BUSINESS, LOSS OF PROFITS, BUSINESS INTERRUPTION, LOSS OF BUSINESS INFORMATION AND THE LIKE) ARISING OUT OF THE USE OF THE INFORMATION CONTAINED IN THIS BULLETIN.*

Section 2 General Information

*Hirose's **IT3** connector system is designed to provide modular high-speed differential, single-ended and power connections between two parallel boards. The interconnection to the PWBs utilizes process-friendly Ball Grid Array receptacles, while the stacking height of 15 to 40mm is set by an impedance-controlled interposer that is added at the system level.*

*The **IT3** connector system consists of two receptacles and one interposer. The receptacles have low profiles and open bodies. The BGA balls are mounted on compliant pins and are set on a staggered grid of 1.5 and 1.75 mm pitch. Both the mating and mounting receptacles' footprints are compatible with popular mezzanine connectors. Receptacles are available in tin-lead and lead-free configurations, and can be used in no-clean or water-wash assembly processes.*

The interposer is an assembly consisting of individual wafers, each carrying 10 signal and 9 ground connections. The interposer is mounted to the receptacles and locked in with mechanical latches to create highly reliable and stable mechanical and electrical connections.

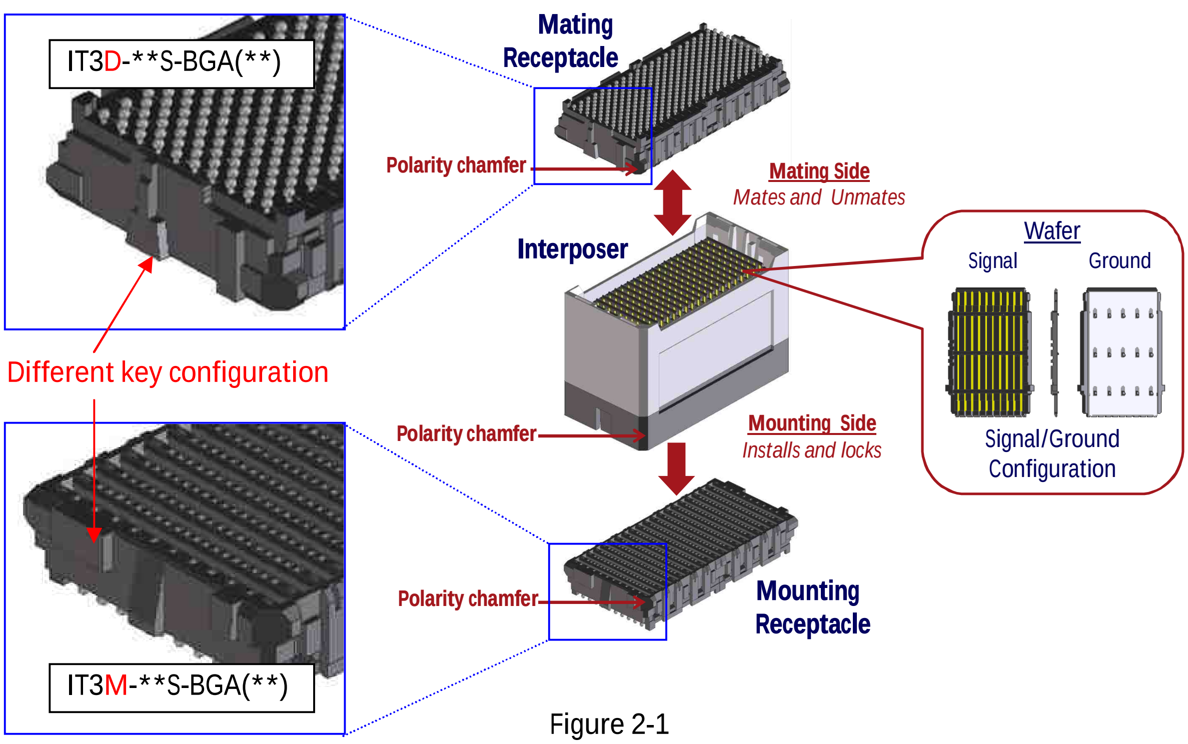
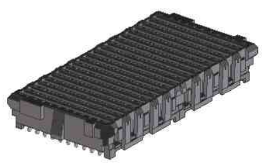
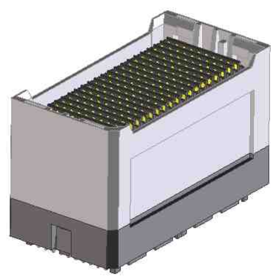


Figure 2-1

This section of the Design Note discusses component weights, part number designation, and general dimensions.

2.1 Component Weights

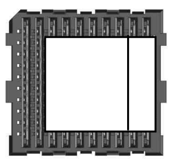
2.1.1 Weight by assembly process

Stacking Height	Receptacle (IT3M) after cap / tape is removed			Receptacle (IT3M) after Interposer is installed			Interposer and two Receptacles (IT3M & IT3D) after final assembly		
									
	Contact position								
	100	200	300	100	200	300	100	200	300
17 mm				9.0 g	15.5 g	22.0 g	11.5 g	20.2 g	28.8 g
18 mm				9.7 g	16.2 g	22.7 g	12.2 g	20.9 g	29.5 g
20 mm				11.0 g	19.4 g	27.7 g	13.5 g	24.1 g	34.5 g
22 mm				12.4 g	19.4 g	31.5 g	13.5 g	24.1 g	38.3 g
25 mm				14.5 g	25.8 g	37.1 g	17.0 g	30.5g	48.3 g
26 mm				15.2 g	27.1 g	39.1 g	17.7 g	31.8 g	45.9 g
28 mm	2.5 g	4.7 g	6.9 g	16.5 g	29.7 g	42.9 g	19.0 g	34.4 g	49.7 g
30 mm				17.9 g	32.3 g	46.7 g	20.4 g	37.0 g	53.5g
32 mm				19.3 g	34.9 g	50.5 g	21.8 g	39.6 g	57.3 g
35 mm				21.4 g	38.8 g	55.0 g	23.9 g	43.5 g	61.8 g
38 mm				23.4 g	42.7 g	59.5 g	25.9 g	47.4 g	66.3 g
40 mm				24.8 g	45.3 g	62.7 g	27.3 g	50.0 g	69.5 g

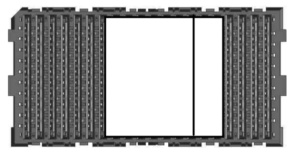
**Components listed in gray letters are under development*

2.1.2 Mating Receptacle with cap or tape

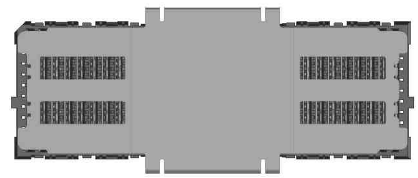
IT3D-100S-BGA



IT3D-200S-BGA



IT3D-300S-BGA

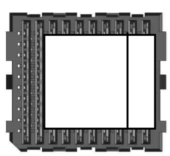


Contact Positions	Part Number	Weight
100 (100 signals/90 grounds)	IT3D-100S-BGA(**)	2.5 g
200 (200 signals/180 grounds)	IT3D-200S-BGA(**)	4.7 g
300 (300 signals/270 grounds)	IT3D-300S-BGA(**)	9.0 g

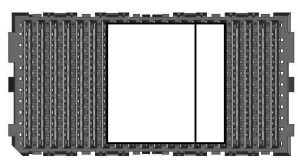
** Receptacle will accept any available stacking height*

2.1.3 Mounting Receptacle with cap or tape

IT3M-100S-BGA



IT3M-200S-BGA

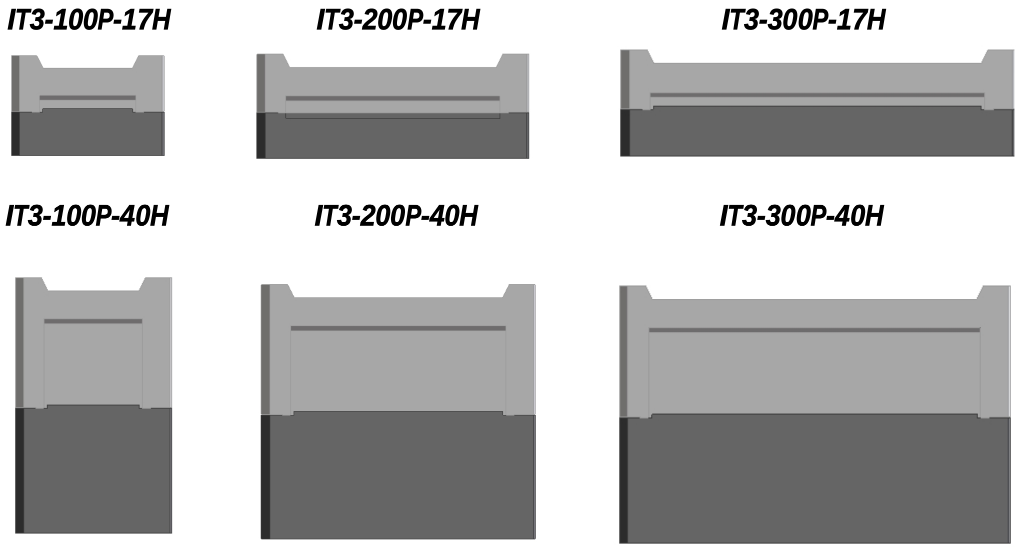


IT3M-300S-BGA

Contact Positions	Part Number	Weight
100 (100 signals/90 grounds)	IT3M-100S-BGA(**)	2.5 g
200 (200 signals/180 grounds)	IT3M-200S-BGA(**)	4.7 g
300 (300 signals/270 grounds)	IT3M-300S-BGA(**)	9.1 g

** Receptacle will accept any available stacking height*

2.1.4 Interposer

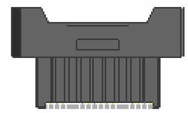


Stacking Height	Contact Position					
	100		200		300	
	Part Number	Weight	Part Number	Weight	Part Number	Weight
17 mm	IT3-100P-17H	6.5 g	IT3-200P-17H	10.8 g	IT3-300P-17H	15.1 g
18 mm	IT3-100P-18H	7.2 g	IT3-200P-18H	12.1 g	IT3-300P-18H	17.0 g
20 mm	IT3-100P-20H	8.5 g	IT3-200P-20H	14.7 g	IT3-300P-20H	20.8 g
22 mm	IT3-100P-22H	9.9 g	IT3-200P-22H	17.3 g	IT3-300P-22H	24.6 g
25 mm	IT3-100P-25H	12.0 g	IT3-200P-25H	21.1 g	IT3-300P-25H	30.3 g
26 mm	IT3-100P-26H	12.7 g	IT3-200P-26H	22.4 g	IT3-300P-26H	32.2 g
28 mm	IT3-100P-28H	14.0 g	IT3-200P-28H	25.0 g	IT3-300P-28H	36.0 g
30 mm	IT3-100P-30H	15.4 g	IT3-200P-30H	27.6 g	IT3-300P-30H	39.8 g
32 mm	IT3-100P-32H	16.8 g	IT3-200P-32H	30.2 g	IT3-300P-32H	43.6 g
35 mm	IT3-100P-35H	18.9 g	IT3-200P-35H	34.6 g	IT3-300P-35H	49.7 g
38 mm	IT3-100P-38H	20.9 g	IT3-200P-38H	38.0 g	IT3-300P-38H	52.6 g
40 mm	IT3-100P-40H	22.3 g	IT3-200P-40H	40.6 g	IT3-300P-40H	55.8 g

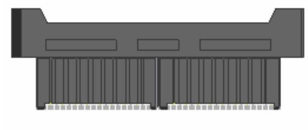
**Components listed in gray letters are under development*

2.1.5 Plug

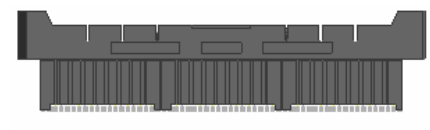
IT3M-100P-15BGA



IT3M-200P-15BGA



IT3M-300P-15BGA



Stacking Height	Contact Positions	Part Number	Weight
14 mm	100 (100 signals/90 grounds)	IT3M-100P-14BGA(**)	6.5 g
	200 (200 signals/180 grounds)	IT3M-200P-14BGA(**)	12.2 g
	300 (300 signals/270 grounds)	IT3M-300P-14BGA(**)	17.7 g
15 mm	100 (100 signals/90 grounds)	IT3M-100P-15BGA(**)	7.0 g
	200 (200 signals/180 grounds)	IT3M-200P-15BGA(**)	12.7 g
	300 (300 signals/270 grounds)	IT3M-300P-15BGA(**)	18.2 g

** Components listed in gray letters are under development*

2.2 Part Number Designation / Manufacturing Lot Number Location

2.2.1 Part Number Designation

Receptacle

IT3xx - xxx S – BGA xx (xx)

(1)(2) (3) (4) (5) (6) (7)

Interposer

IT3xx - xxx P – xxH xx (xx)

(1)(8) (3) (4) (9) (6) (10)

Plug

IT3Mx - xxx P – xxBGA xx (xx)

(1)(2) (3) (4) (9) (5) (6) (7)

(1) Series name: *IT3*

No Further Designation

(2) Receptacle Type

IT3D-xxxS-BGA: Mating Receptacle
IT3Dx-xxxS-BGA: Mating Receptacle (Customized)
IT3M-xxxS-BGA : Mounting Receptacle
IT3Mx-xxxS-BGA: Mounting Receptacle (Customized)
IT3M-xxxP-xxBGA : Plug
IT3Mx-xxxP-xxBGA: Plug (customized)

(3) Contact Positions

100, 200, 300

(4) Connector

S : Socket
P : Plug

(5) BGA: Ball Grid Array

No Further Designation

(6) Package Specification

Blank: Standard
xx: Customized

(7) Material and Plating Specification of Receptacle

(37): Pb-free Solder: Sn (96.5) Ag (3.0) Cu (0.5)
Contact Area: Gold(0.76 µm)+Ni(1.5 µm)
(39): Pb-free Solder: Sn (96.5) Ag (3.0) Cu (0.5)
Contact area: Gold(0.76 µm)+Ni(1.5 µm)
(D-side receptacle only) housing color: gray
(57): Eutectic Solder: Sn (63) Pb (37)
Contact Area: Gold(0.76 µm)+Ni(1.5 µm)
(59): Eutectic Solder: Sn (63) Pb (37)
Contact Area: Gold(0.76 µm)+Ni(1.5 µm)
(D-side receptacle only) housing color: gray

(8) Interposer Type

Blank: Standard
xx: Customized

(9) Stacking Height (mm)

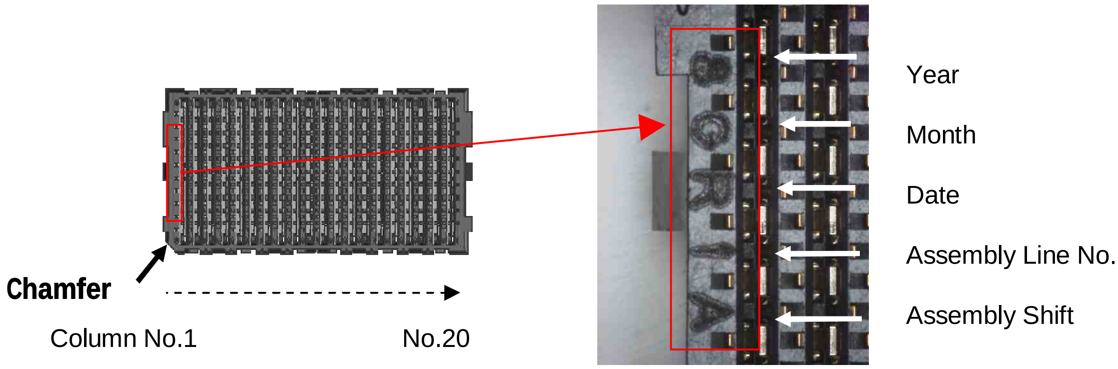
14, 15, 17, 18, 20, 22, 25, 26, 28, 30, 32, 35, 38, 40

(10) Plating Specification of Interposer

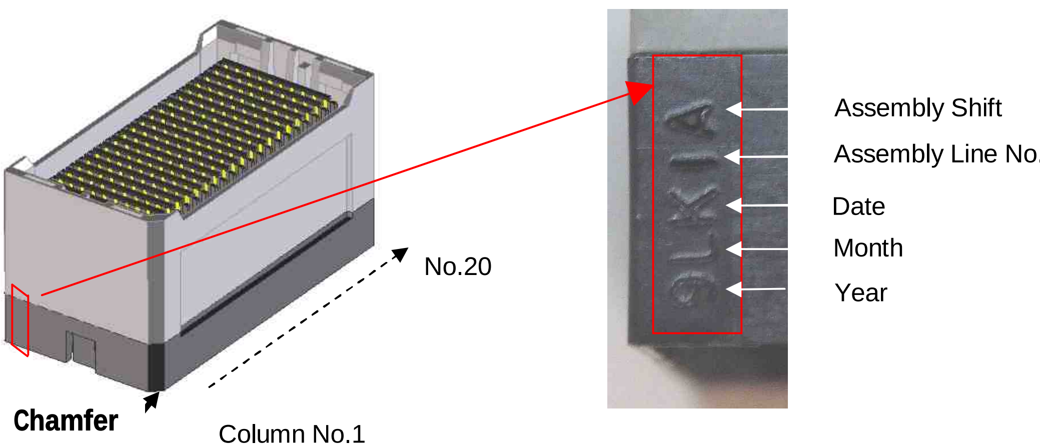
(03): Contact Area: Gold(0.76 µm)+Ni(1.5 µm)

2.2.2 Manufacturing Lot Number

Receptacle (Ex. 200pos)

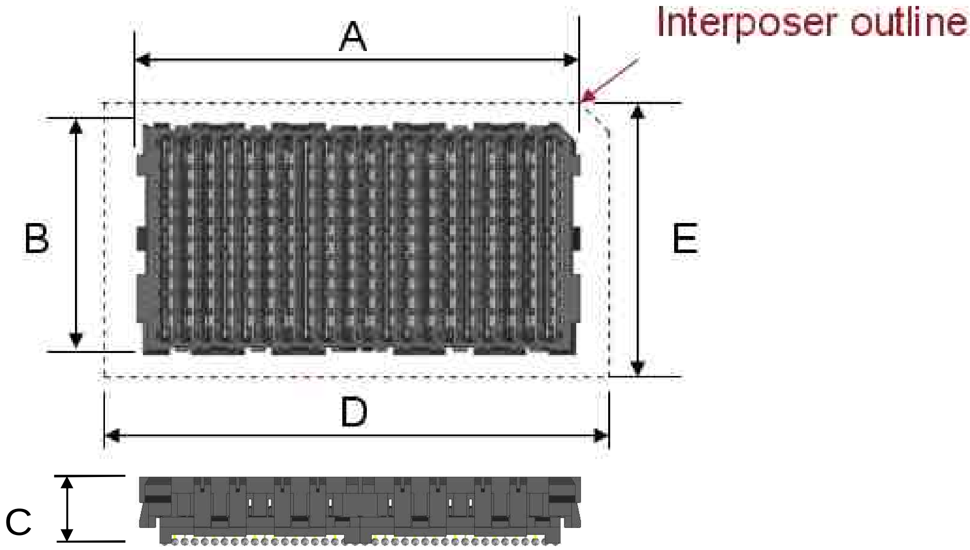


Interposer (Ex. 200pos)



* Lot number indication may subject to change.

2.3 Receptacle General Dimensions



Shown: 200 position mating receptacle, IT3M-200S-BGA

		Contact Position		
		100	200	300
No. of Signal Contacts		100	200	300
No. of Ground Contacts		90	180	270
A	Receptacle Length	21	38.5	56
B	Receptacle Width	19.2	19.2	19.2
C	Receptacle Height	6	6	6
D	Interposer/Plug Outline Length	24	41.5	59
E	Interposer/Plug Outline Width	21	21	21

**All dimensions shown are in mm*

Section 3 Operating Characteristics

This section of the Design Note discusses material, electrical, mechanical, and environmental characteristics. It also discusses BGA reliability testing.

3.1 Material

Numbering of component is same as customer drawing.

3.1.1 Receptacle

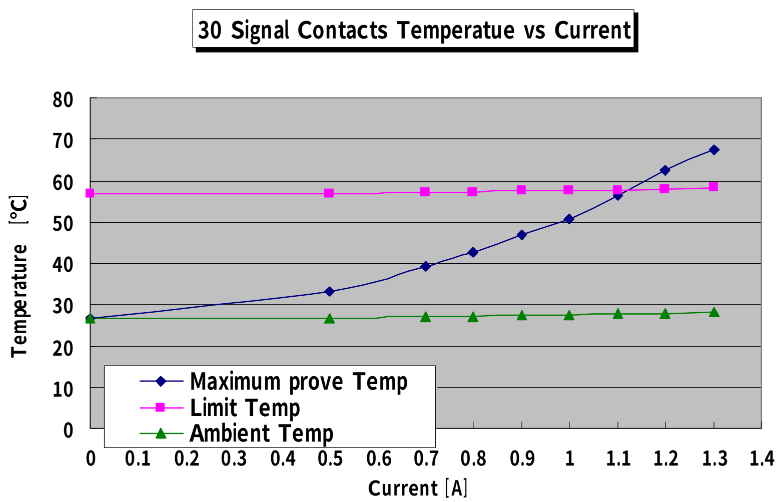
NO	Component	Material	Finish & Remarks
1	Housing	LCP	Black or Gray, UL 94V-0
2	Locator	LCP	Black , UL 94V-0
3	Contact	Copper Alloy	Contact Area : Gold (0.76 micron) over Nickel (1.5 micron) Mounting Area : Gold (0.03 micron) over Nickel (1.5 micron) Other : Nickel (1.5 micron)
4	Solder Ball	Tin-Lead (SnPb)	Sn(63)-Pb(37)
		Tin (Pb-Free)	Sn(96.5)-Ag(3)-Cu(0.5)
5	Tray	Polystyrene	Black
6	Pick Up Cap	Stainless steel	300pos
	Pick Up Tape	Paper(Nomex)	100pos and 200pos

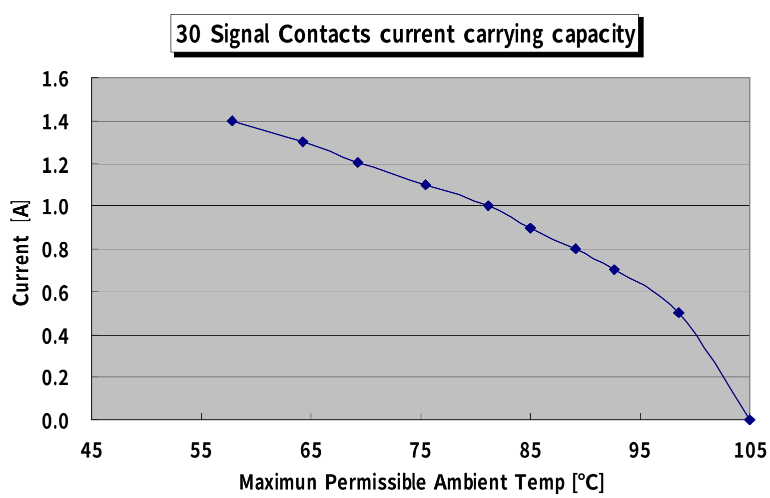
3.1.2 Interposer

NO	Component	Material	Finish & Remarks
1	Guide(Mounting Side)	PBT	Black , UL 94V-0
2	Guide(Mating Side)	LCP	Gray , UL 94V-0
		PBT	Gray , UL 94V-0
3	Blade	LCP	Black , UL 94V-0
4	Contact	Copper Alloy	Contact Area : Gold (0.76 micron) over Nickel (1.5 micron) Other : Nickel (1.5 micron)
5	Ground Shield	Copper Alloy	
6	Tray	Polypropylene	—

3.2 Electrical

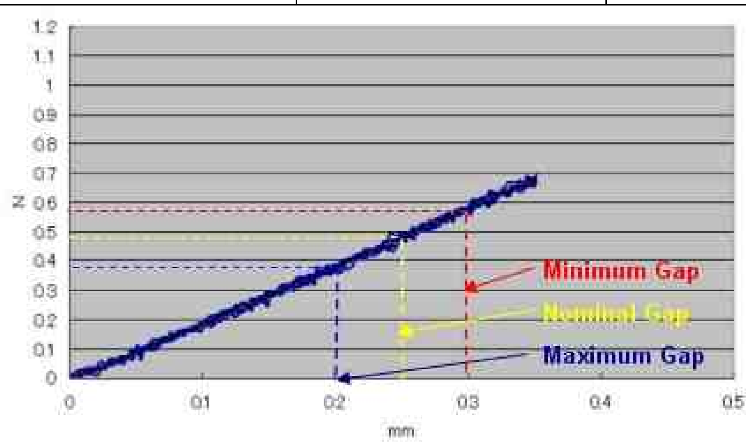
Test	Test Condition	Requirement	Typical Value
Low Level Contact Resistance* (LLCR)	EIA-364-23	50 mohm MAX (15 - 24 H) 55 mohm MAX (25 - 32 H) 60 mohm MAX (33 - 40 H) (H : stacking height in mm)	20-25 mohm (15 - 24 H) 25-30 mohm (25 - 32 H) 30-35 mohm (33 - 40 H) (H : stacking height in mm)
Insulation Resistance (IR)	EIA-364-21	1000M ohm MIN	Over 20,000M ohm
Dielectric Withstanding Voltage (DWV)	EIA-364-20 AC 150V for 60 seconds Different contacts than LLCR	No disruptive discharge No leakage current : 2mA MAX	Break voltage: over 800V
Current Rating	EIA-364-70	30°C temperature rise	Signal contact : 1A / pin
	Fore more detailed information, see TR0636E-20041 “Temperature rise test report”.		





***** The value of contact resistance includes 2 contact points and the bulk resistance

3.3 Mechanical

Test	Test Condition	Requirement	Typical Value
Mating / Unmating Force	EIA-364-13	Mating : 45 N MAX (100pos) 90 N MAX (200pos) 135 N MAX (300pos) Unmating : 5N MIN (100pos) 10N MIN (200pos) 15N MIN (300pos)	Mating : 35 N (100pos) 70 N (200pos) 105 N (300pos) Unmating : 20N (100pos) 35N (200pos) 55N (300pos)
Durability	EIA-364-09 Cycle rate : 300 maximum per hour 100 times (mating side) 5 times (mounting side)	No evidence of physical damage	-
Random Vibration	EIA-364-28, Condition V, letter D 90 min in each 3 directions Electrical lord condition : 100mA max	Less than 1micro second	-
Sinusoidal Vibration	GR1217 Section 9.1.2.1 EIA-364-28B, condition II 10-500Hz in each 3 directions 2H 10G	Less than 1micro second	-
Mechanical Shock	GR1217 Section 9.1.2.1 EIA-364-27, condition I 3 directions each, 50G, 11ms, 18 times	Less than 1micro second	-
Packing	ISTA-3A	No evidence of physical damage BGA co-planarity: 0.18mm max	-
Contact Normal Force	-	0.3N min	0.45N
			
Contact Wiping Length	1.4+/-0.3 mm (without recommended spacers) 1.0+/-0.3 mm (with recommended spacers) Refer to page 49 for recommended spacer information		-
Contact Retention Force	1.5N min / signal contact		-
BGA Co-planarity	0.18 mm Max		-

3.3.1 Cross Section

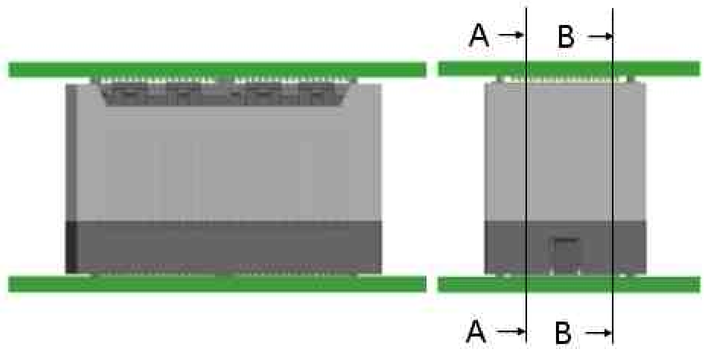
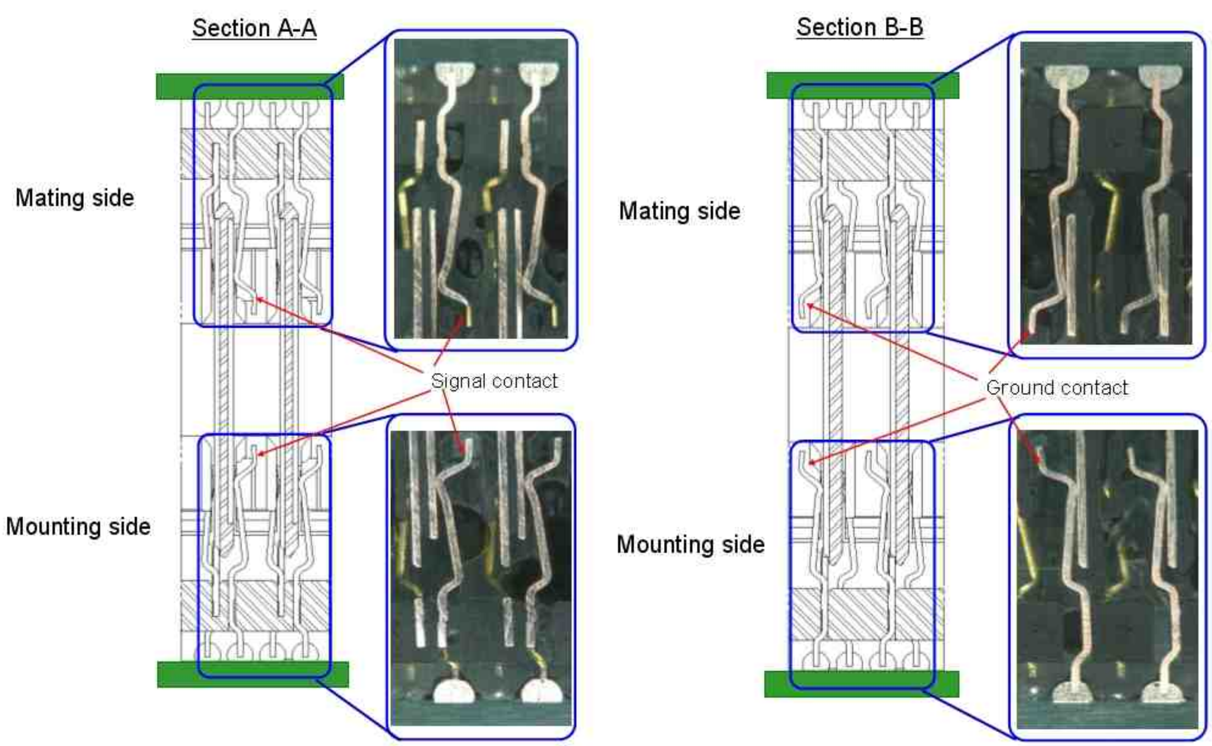


Figure 3-1

Signal contact

Ground contact



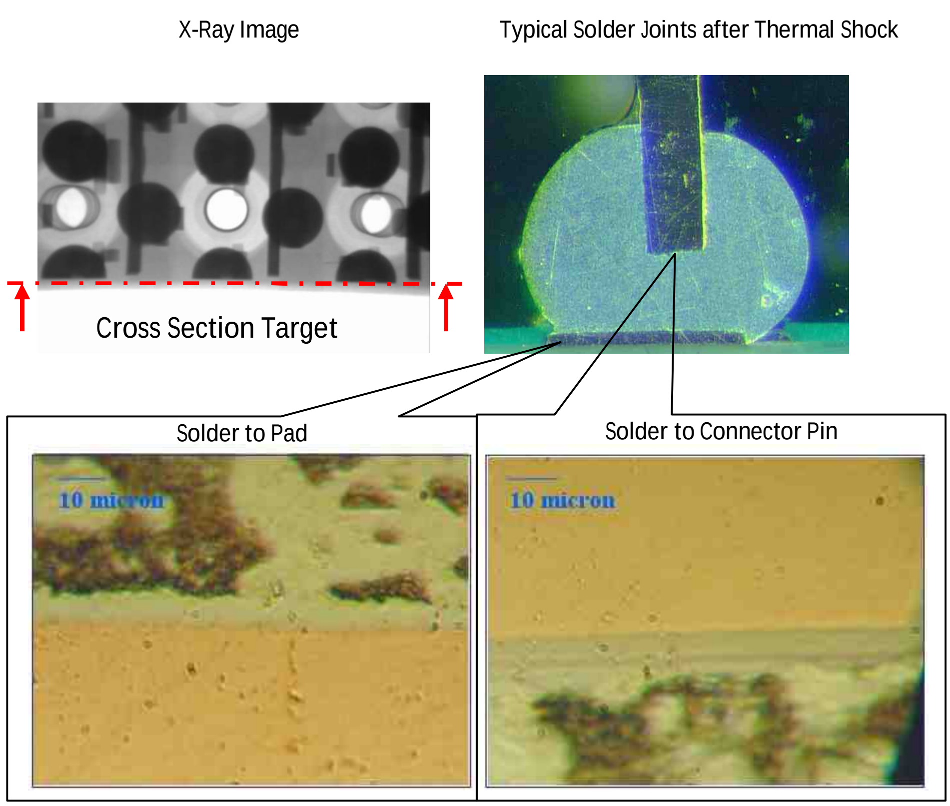
3.4 Environmental

We guarantee 10 years of storage per satisfactory results from accelerated high temperature tests that store connectors at 105 °C for more than 120 hours according to EIA-364-1000.01. The specification has Table 8 - Test durations (hours) for temperature life which indicates the previously-mentioned accelerated test condition equal to 60 °C (typical maximum temperature for office environment set by one of our major customers) for 10 years.
The performance of our connectors is satisfactory within an environmentally-related corrosive atmosphere according to EIA-364-65. Test procedure that covers this specification allows the observation of how plated and unplated surfaces react when exposed to different concentrations of flowing gas mixtures.

Test	Test Condition	Requirement	Remarks
Thermal Shock	EIA-364-32 Condition 1 -55 to 85 °C, 10cycles Recovery : 1/2 hour minimum	No evidence of physical damage Resistance change: 20 milli-ohms MAX	-
Cyclic Temperature & Humidity	EIA-364-31, EIA-364-1000.01, Table 2 Conditioning : dry oven at 50 °C, 24h Rest condition : see Appendix 2 Recovery : 5 h	No evidence of physical damage Resistance change: 20 milli-ohms MAX	-
Humidity	EIA-364-31 condition A 500h , 90-95% , 42 +/-2 °C	No evidence of physical damage Resistance change: 20 milli-ohms MAX	-
Temperature Life	EIA-364-17, Method A, condition 3 85 °C, 500h	No evidence of physical damage Resistance change: 20 milli-ohms MAX	-
Cold	IEC-60512-11-10 (JIS C 5402 7.9) -55 °C, 96h	No evidence of physical damage Resistance change: 20 milli-ohms MAX	-
Salt Spray	IEC-60512-11-6 (JIS C 5402 7.1) Salt 5 wt% , 35 °C, 48h	No evidence of physical damage Resistance change: 20 milli-ohms MAX	-
Mixed Flowing Gas	EIA-364-65, Class IIA Concentration (ppb) Cl2 : 10±3 NO2 : 200±50 H2S : 10±5 SO2 : 100±20 RH% : 70±2 Temp °C : 30±1 Exposure : 14days (Unmated 7days, mated 7days) Recovery : 2hrs minimum	No defect such as corrosion which impairs the function of connector Resistance change: 20 milli-ohms MAX	-

3.5 BGA Reliability

These tests apply to both eutectic and lead free applications.

Test	Test Condition	Requirement	Remarks
Thermal Shock	IPC-9701 6000 cycles between 0 and 100 °C	No more than 20% increase from the initial resistance while monitored for five consecutive reading scans	-
Solder Ball Shearing	IPC-9701, 6000 cycles between 0 and 100 °C Shearing speed is 500 mm / second	No inter metallic failure between contacts and balls	-
High Temperature Storage	Refer to IPC-9701, 105 °C, 1000 hours	No more than 20% increase from the initial resistance while monitored for five consecutive reading scans	-
Cross Section	IPC-9701 6000 cycles between 0 and 100 °C	SnCu inter-metallic layers observed at 'Solder to Connector Pin' interface, and at 'Solder to Pad' interface	-
			

Section 4 Signal Integrity

This section of the Design Note the overview, 20Gbps solution, differential and single-ended performance, and propagation delay on Hirose's IT3 signal integrity performance.

4.1 Overview

By meeting the stringent (extrapolated) insertion-loss-to-crosstalk-ratio (ICR) specifications as defined in the IEEE802.3ap standard, IT3 is fully capable of supporting 6.25, 10, or 20 Gbps differential data transmission.

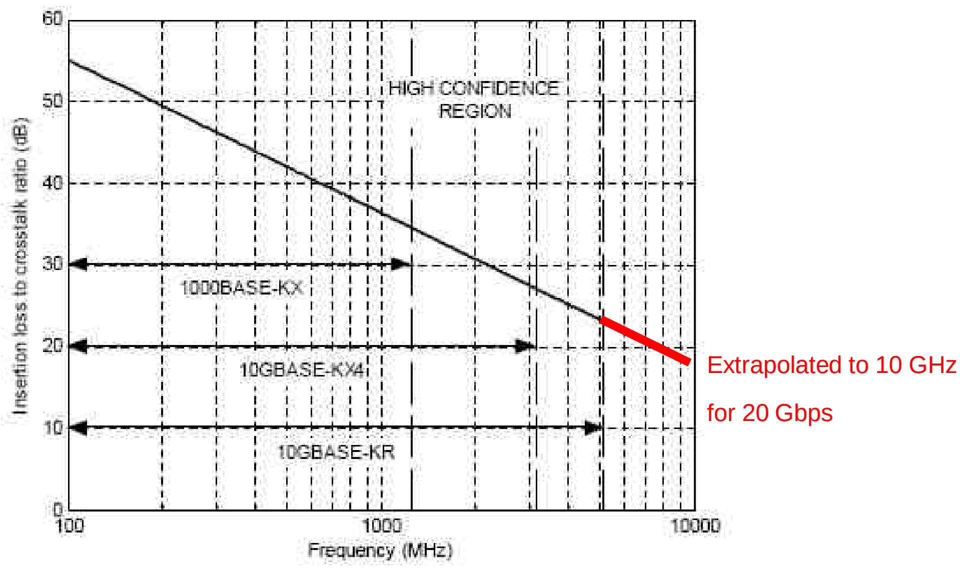


Figure 4-1

For high-speed data transmission, the transmitters (TX) and receivers (RX) are usually grouped separately, in order to minimize the effect of near-end crosstalk (NEXT). Actual measurements were taken on 120mil test boards (Figure 4-2) with IT3-25mm connector, 2 via transitions through mid routing layers, and 6"+6" FR408 PCB traces.

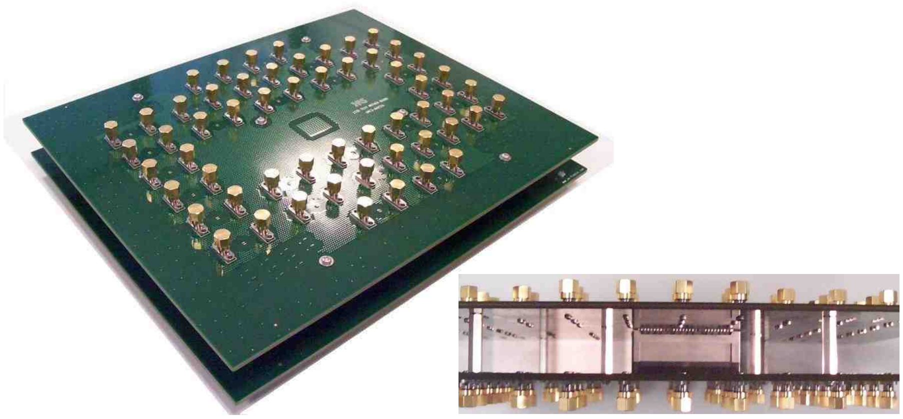


Figure 4-2 Demo board

The following ICR curve (Figure 4-3) corresponds to the power sum of far-end crosstalk (FEXT) from 14 aggressor pairs and 1 victim pair in 3 connector columns. It is clear that IT3 meets the ICR spec. for 6.25 Gbps data rate in a fully-populated configuration (Figure 4-4).

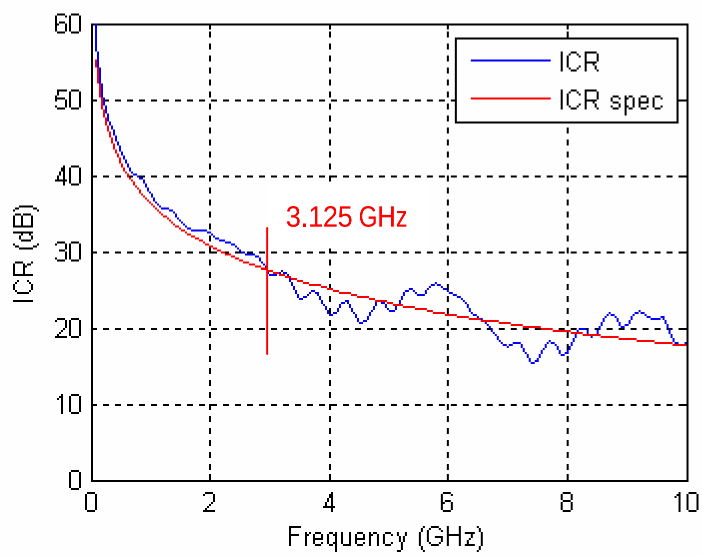


Figure 4-3

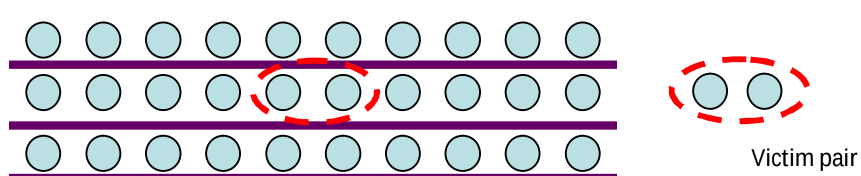


Figure 4-4 Fully-populated pin configuration

4.2 20Gbps Solution

Under the same setup, IT3 meets the extrapolated ICR spec. for 20 Gbps data rate (Figure 4-5) if 40% of pins are "skipped" (Figure 4-6). Skipped pins can be either terminated or assigned to low-speed signals. To avoid resonance, grounding or floating skipped pins is not recommended.

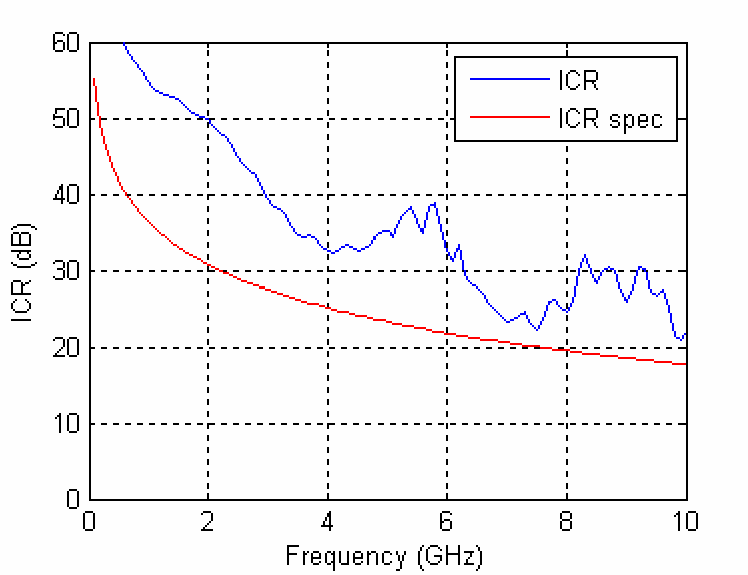


Figure 4-5

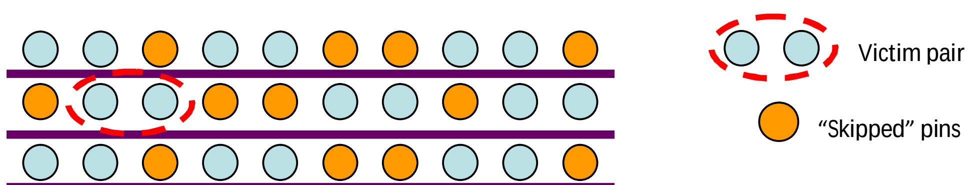


Figure 4-6 Pin configuration with 60% density

4.3 Differential Signals

To examine the behavior of the IT3 connector by itself, 62mil characterization boards were measured with their 1.6" lead-in traces de-embedded.

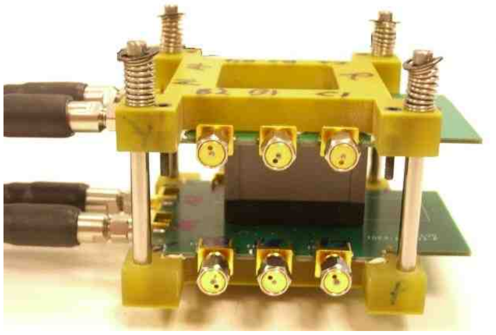


Figure 4-7 Characterization board

Figures 4-9 to 4-11 show the measured vs. simulated differential insertion loss (IL), return loss (RL), near-end crosstalk (NEXT), and far-end crosstalk (FEXT) between two nearest neighbors in an IT3-25mm connector (Figure 4-8). Data at other stack heights are detailed in Section 4.5.

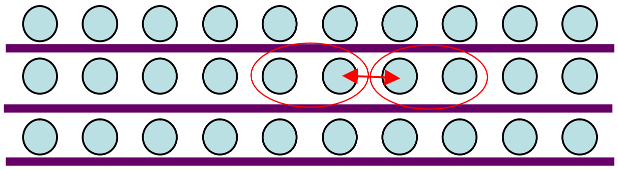


Figure 4-8

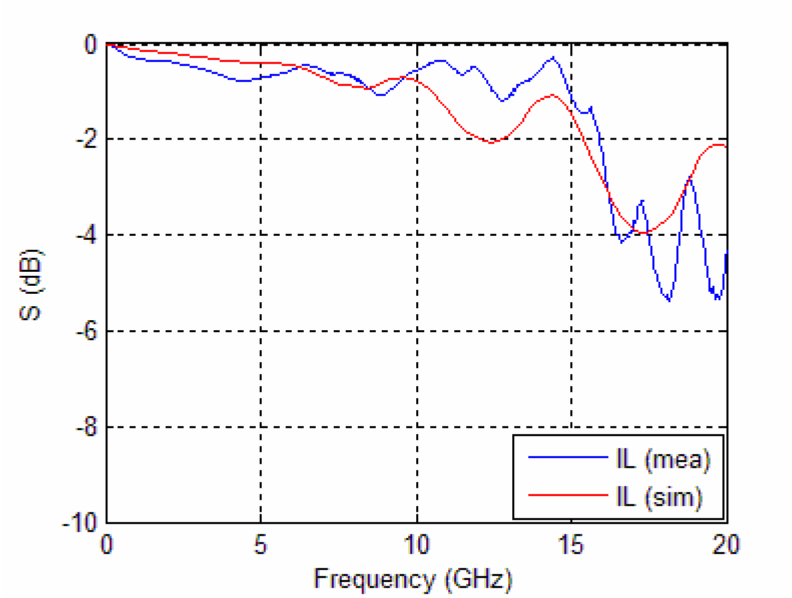


Figure 4-9 Differential insertion loss

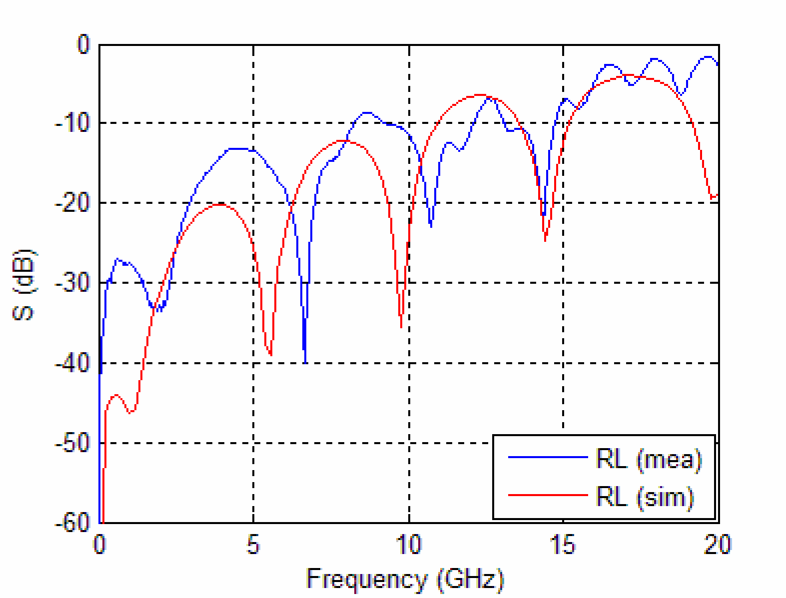


Figure 4-10 Differential return loss

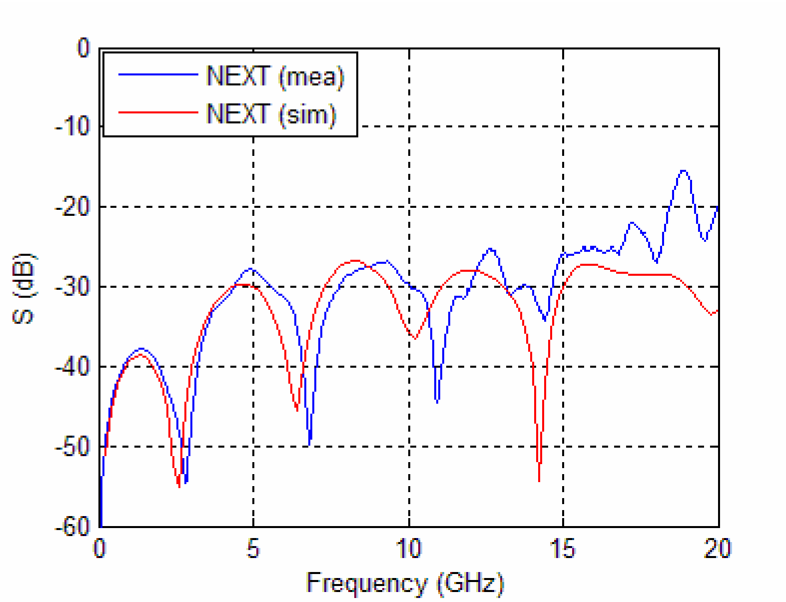


Figure 4-11 Differential NEXT

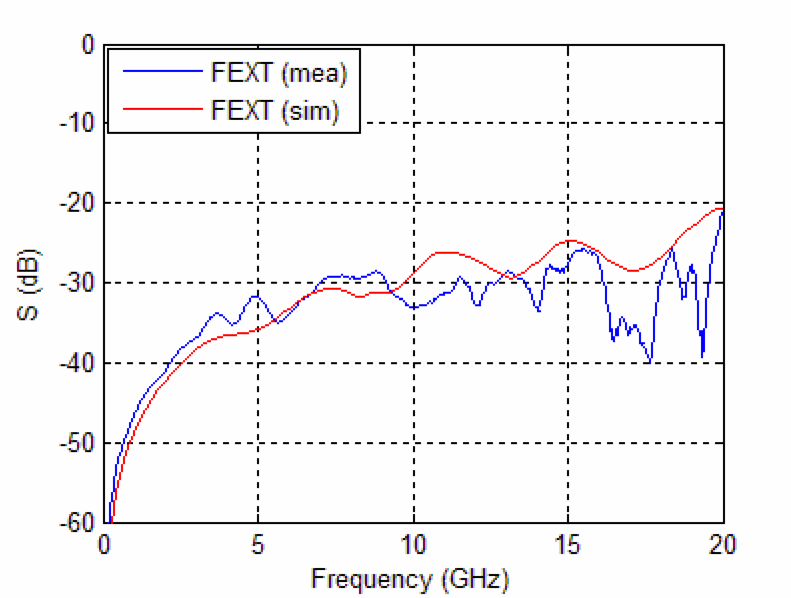


Figure 4-12 Differential FEXT

Figures 4-14 and 4-15 show the simulated NEXT and FEXT among various differential pairs of an IT3-25mm connector in a fully-populated configuration (Figure 4-13).

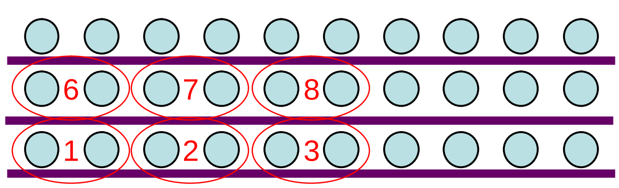


Figure 4-13

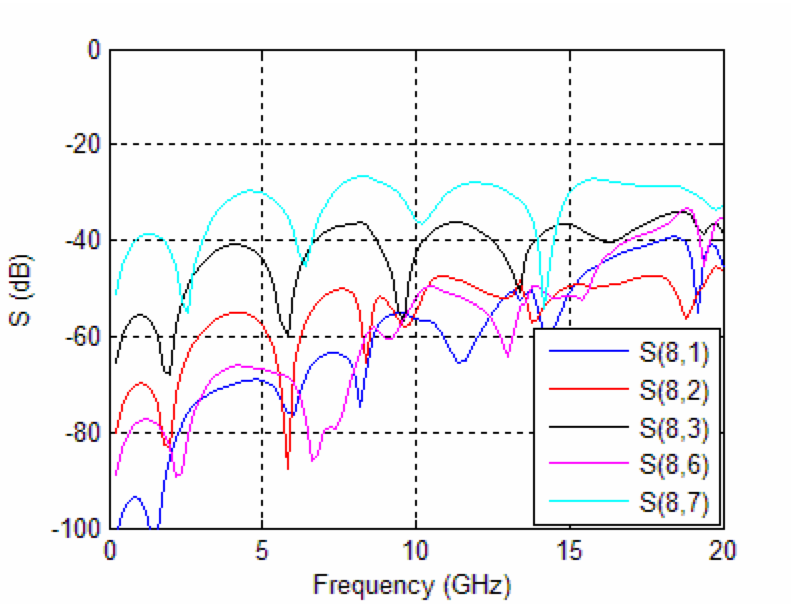


Figure 4-14 Differential NEXT

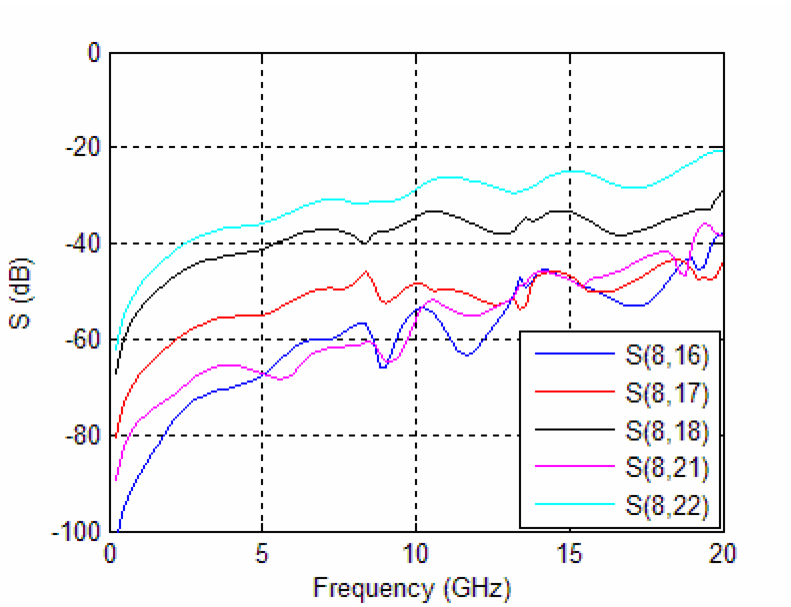


Figure 4-15 Differential FEXT

Figure 4-16 shows the impedance profile of IT3-25mm connector at 30ps (20% to 80%) rise time. Note that IT3's sockets have slightly higher impedance by design, in order to compensate the generally low-impedance vias.

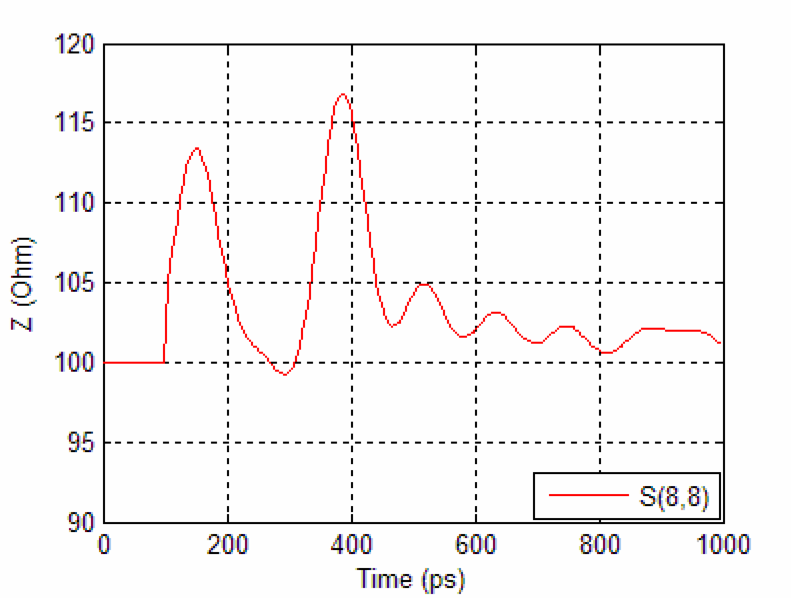


Figure 4-16 Differential impedance

Figures 4-18 and 4-19 show the simulated NEXT and FEXT among various differential pairs of an IT3-25mm connector in a 60% density configuration (Figure 4-17).

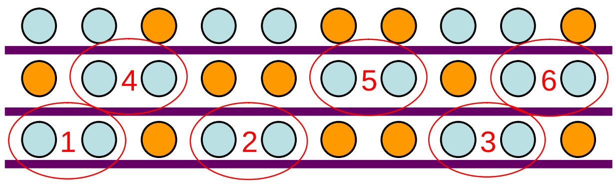


Figure 4-17

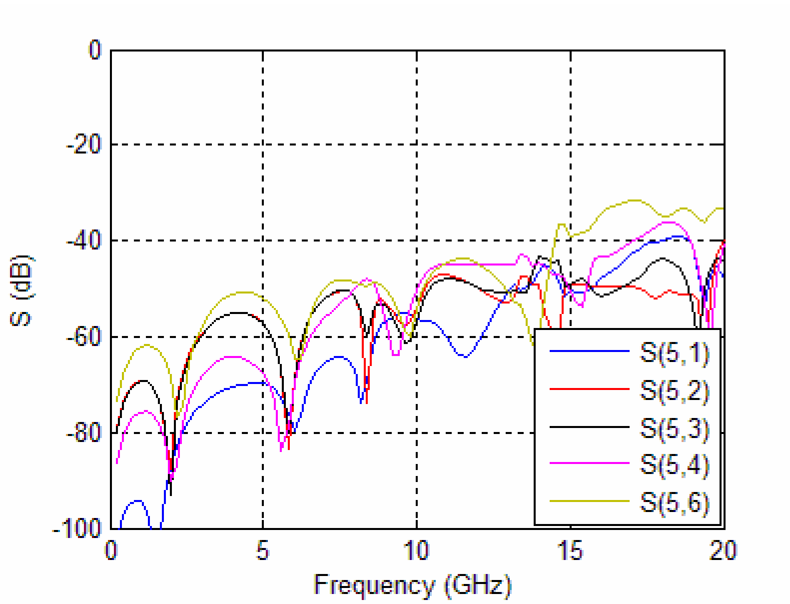


Figure 4-18 Differential NEXT

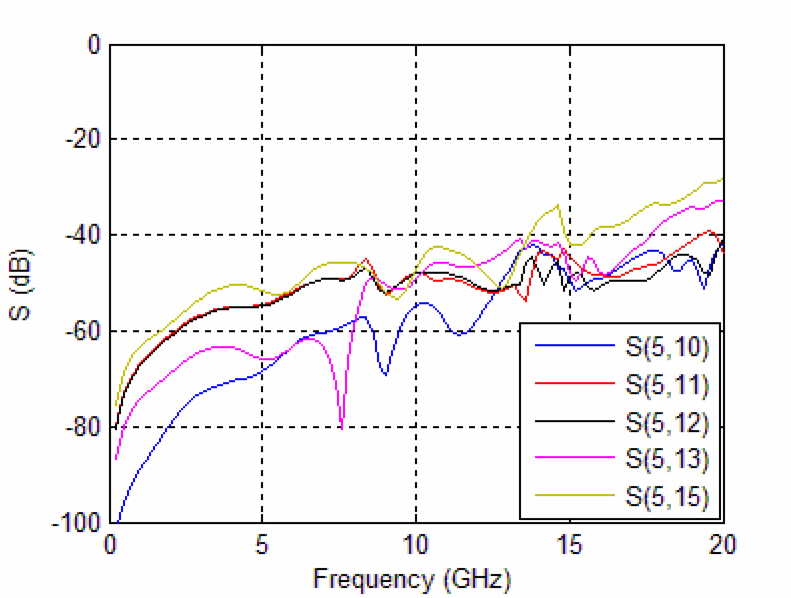


Figure 4-19 Differential FEXT

4.4 Single-ended Signals

Figures 4-21 to 4-23 show the measured vs. simulated single-ended insertion loss (IL), return loss (RL), near-end crosstalk (NEXT), and far-end crosstalk (FEXT) between two nearest neighbors in an IT3-25mm connector (Figure 4-20). Data at other stack heights are detailed in Section 4.6.

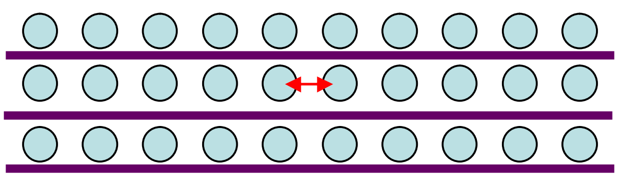


Figure 4-20

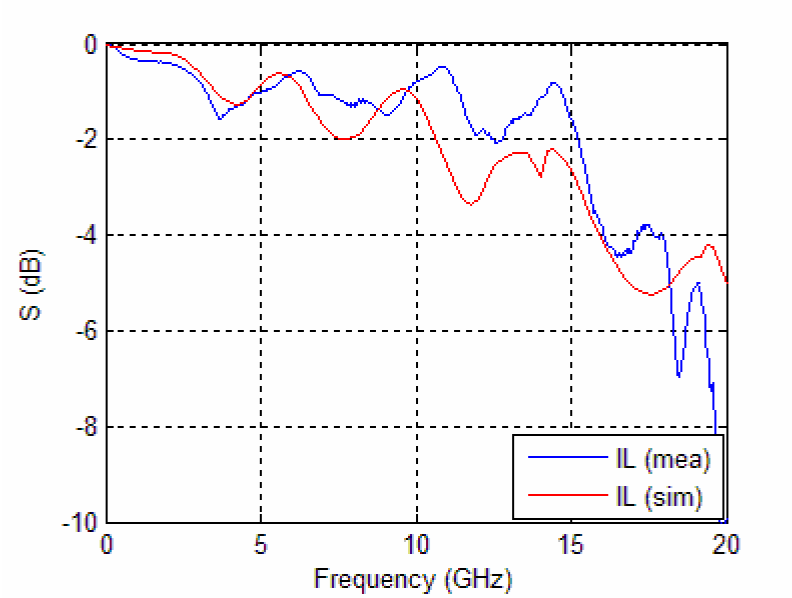


Figure 4-21 Single-ended insertion loss

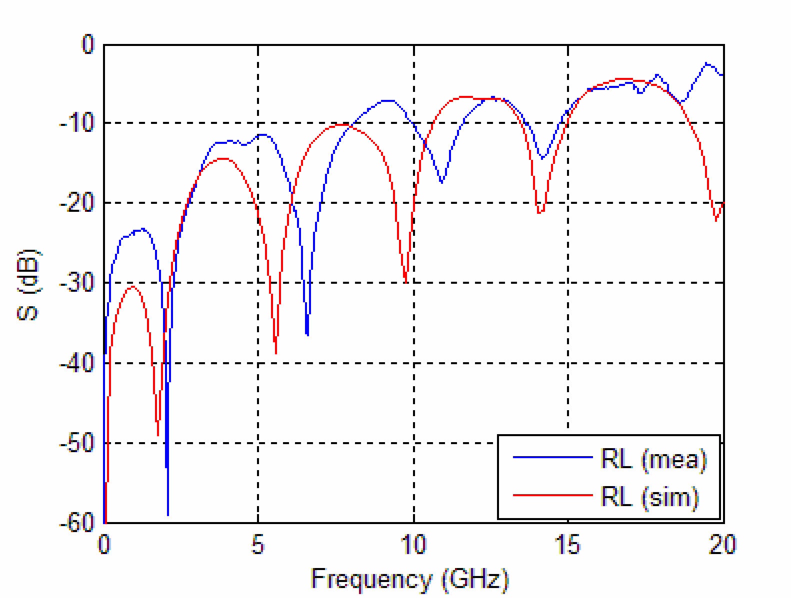


Figure 4-22 Single-ended return loss

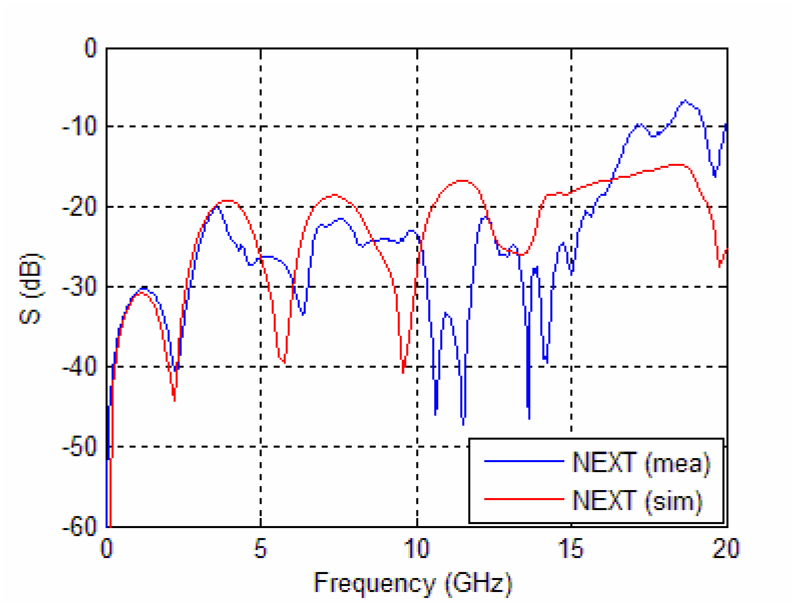


Figure 4-23 Single-ended NEXT

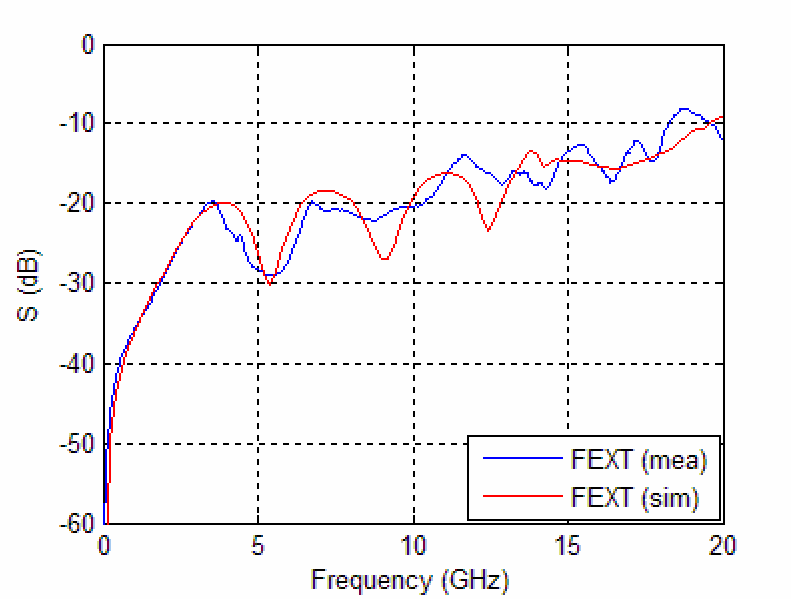


Figure 4-24 Single-ended FEXT

Figures 4-26 and 4-27 show the simulated NEXT and FEXT among various single-ended signals of an IT3-25mm connector in a fully-populated configuration (Figure 4-25).

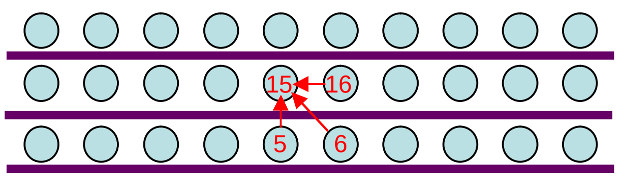


Figure 4-25

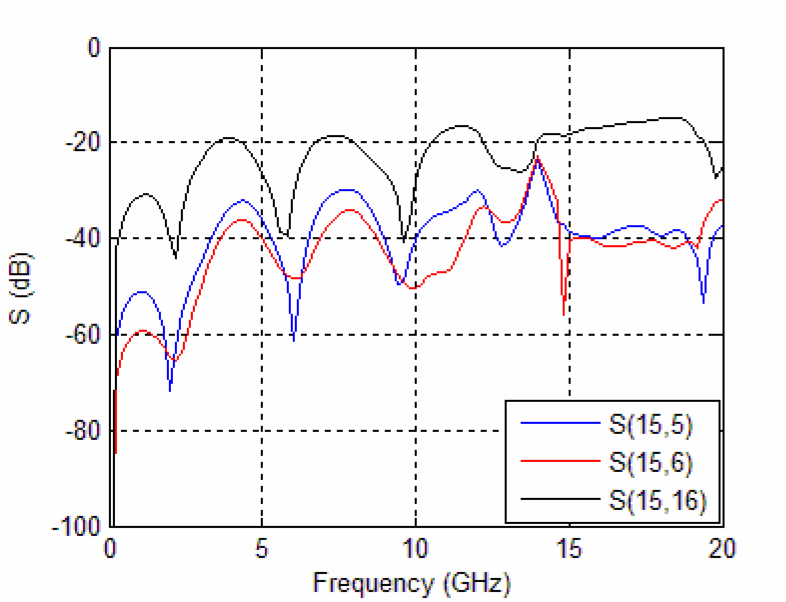


Figure 4-26 Single-ended NEXT

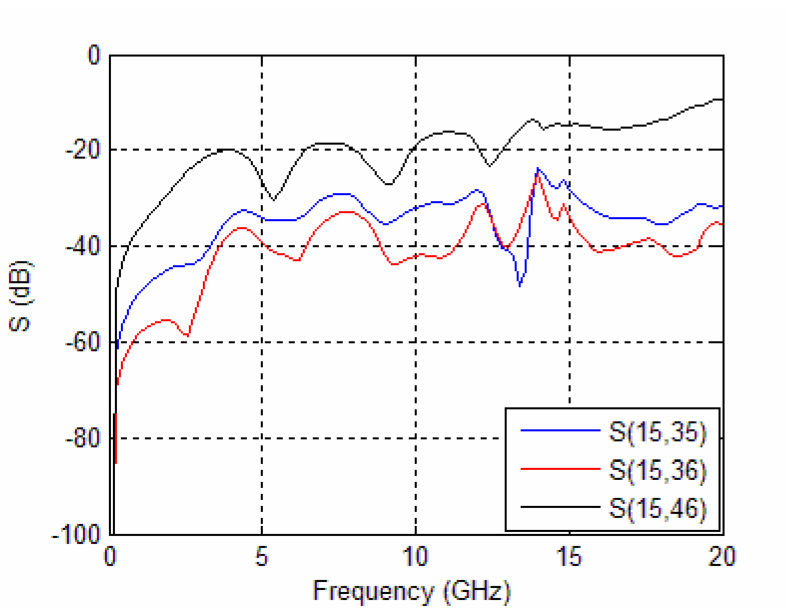


Figure 4-27 Single-ended FEXT

Figures 4-28 to 4-30 show the impedance profile, NEXT, and FEXT of IT3-25mm connector at 200ps (20% to 80%) rise time. Note that IT3's sockets have slightly higher impedance by design, in order to compensate the generally low-impedance vias.

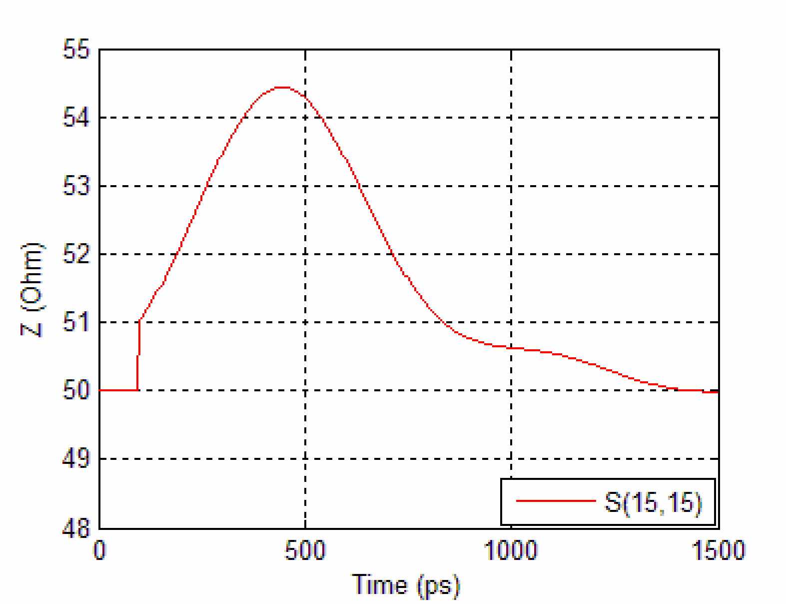


Figure 4-28 Single-ended impedance

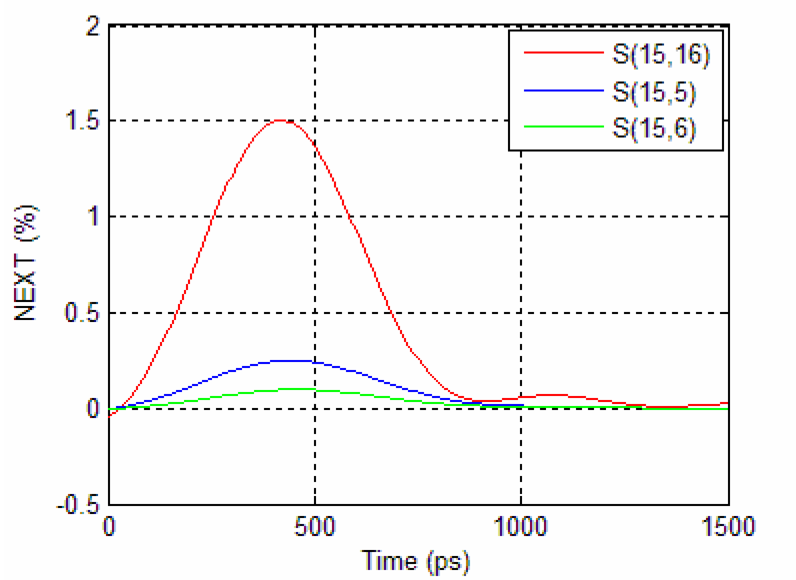


Figure 4-29 Single-ended NEXT

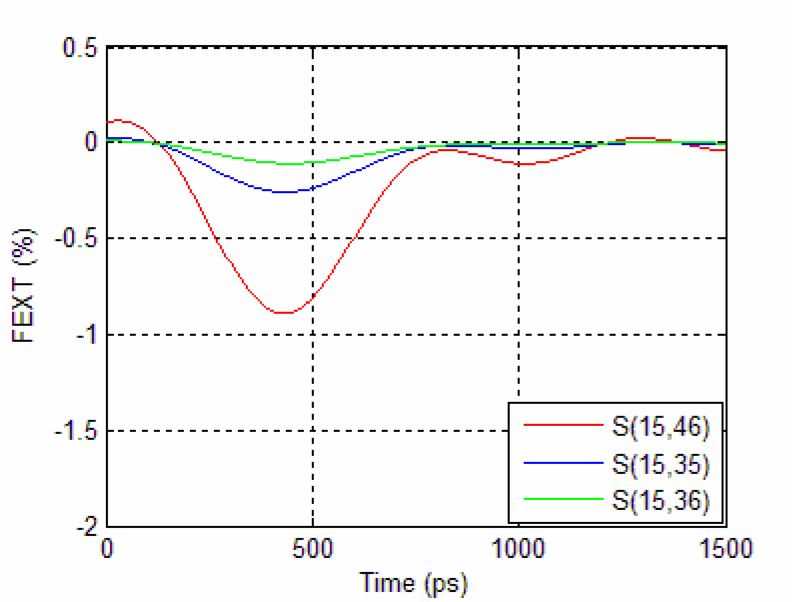


Figure 4-30 Single-ended FEXT

4.5 Differential S Parameters of 17, 26 and 32 mm Height

Figures 4-32 to 4-34 show the measured differential insertion loss, return loss, NEXT, and FEXT for IT3 of 17mm, 26mm, and 32mm stack heights.

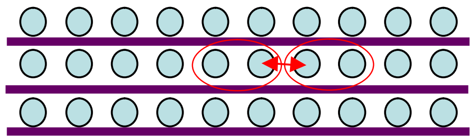


Figure 4-31 (NEXT and FEXT)

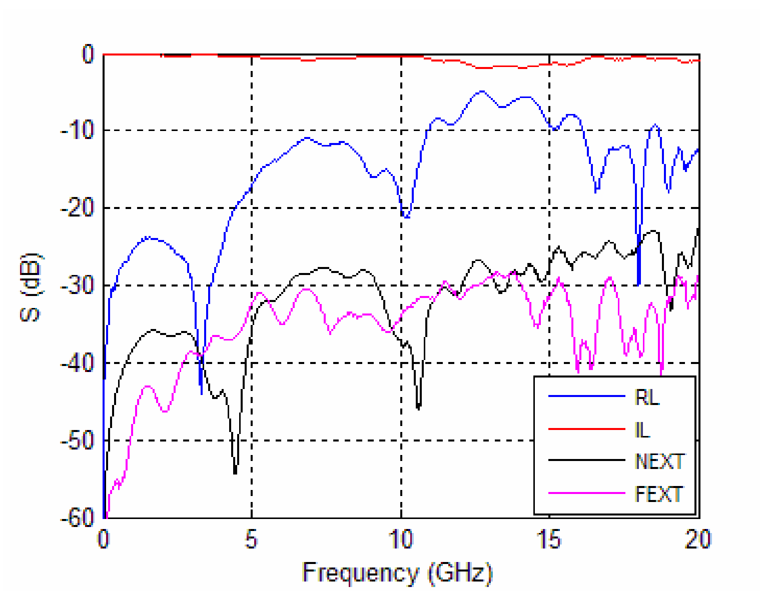


Figure 4-32 Measured differential response for IT3-17mm

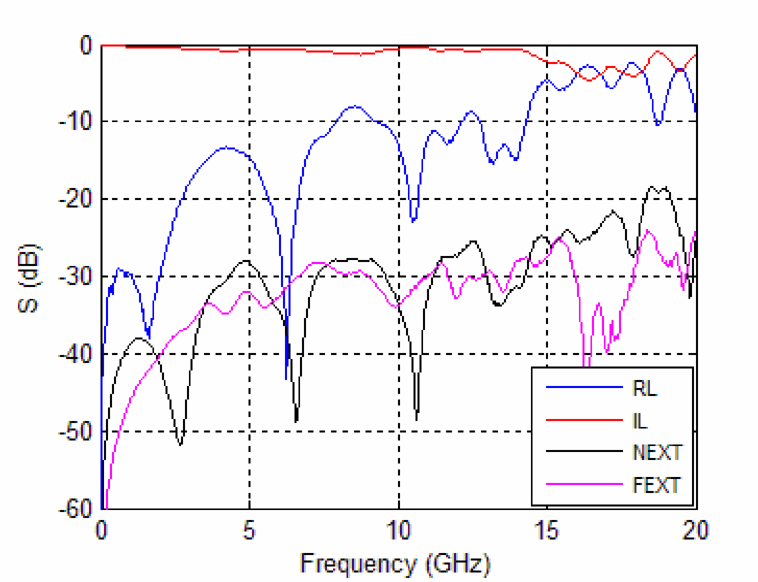


Figure 4-33 Measured differential response for IT3-26mm

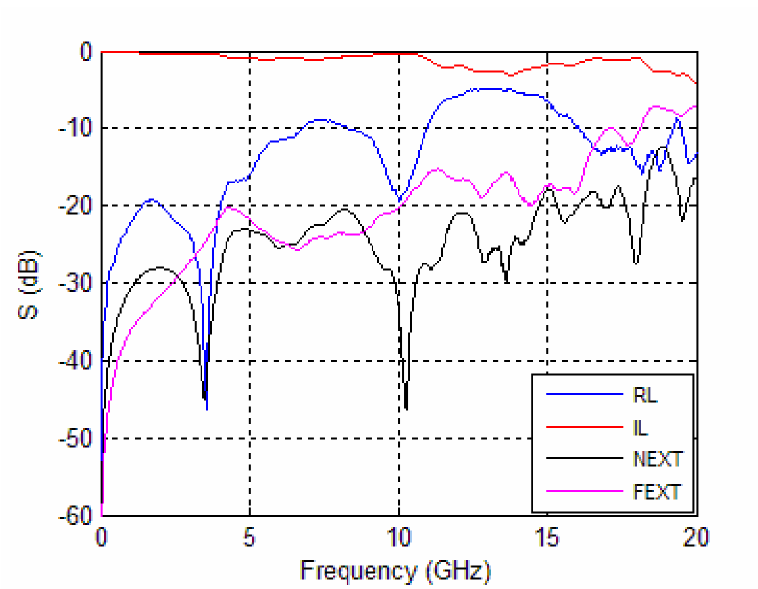


Figure 4-34 Measured differential response for IT3-32mm

4.6 Single-ended S Parameters of 17, 26 and 32 mm Height

Figures 4-36 to 4-38 show the measured differential insertion loss, return loss, NEXT, and FEXT for IT3 of 17mm, 26mm, and 32mm stack heights.

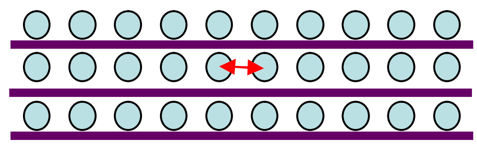


Figure 4-35 (NEXT and FEXT)

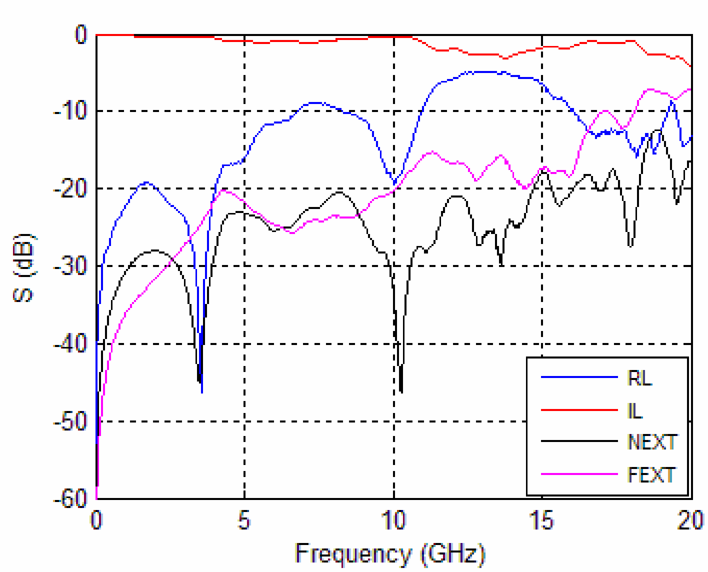


Figure 4-36 Measured single-ended response for IT3-17mm

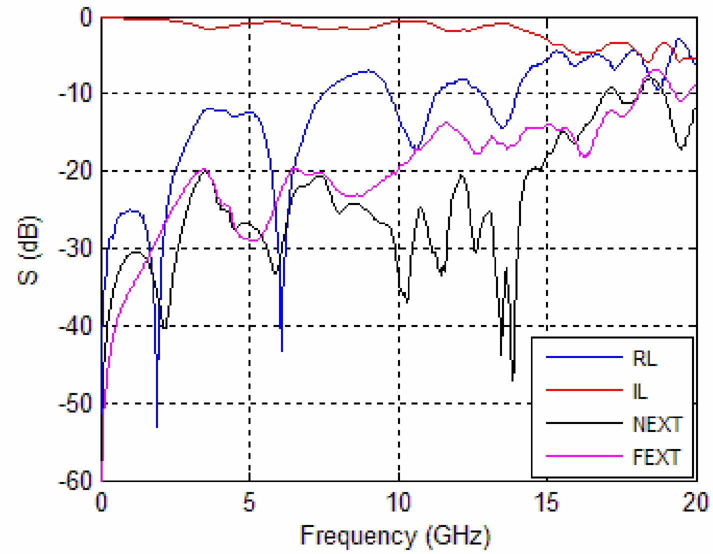


Figure 4-37 Measured single-ended response for IT3-26mm

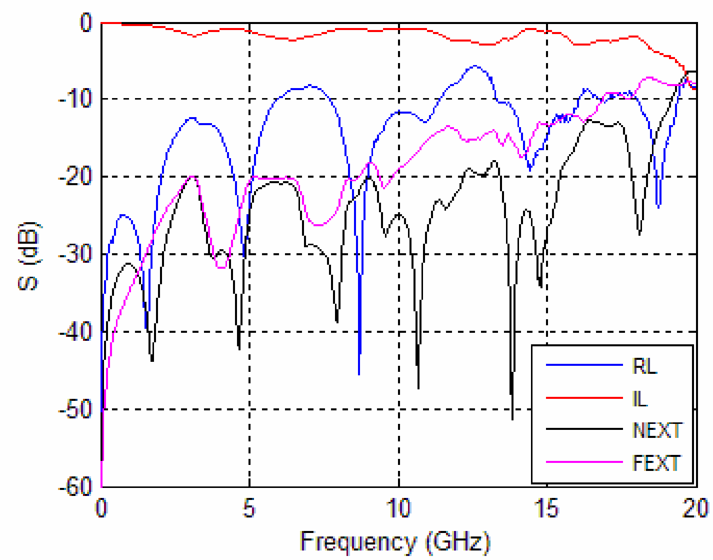


Figure 4-38 Measured single-ended response for IT3-32mm

4.7 Propagation Delay

The following table shows the simulated propagation delay through IT3 connector at 1 GHz.

Stack Height (mm)	Propagation Delay (ps)	
	Differential	Single-Ended
17	101.05	101.59
25	146.69	147.60
26	151.95	153.38
32	188.48	190.08

Table 4-1 Propagation delay

Section 5 PWB Design

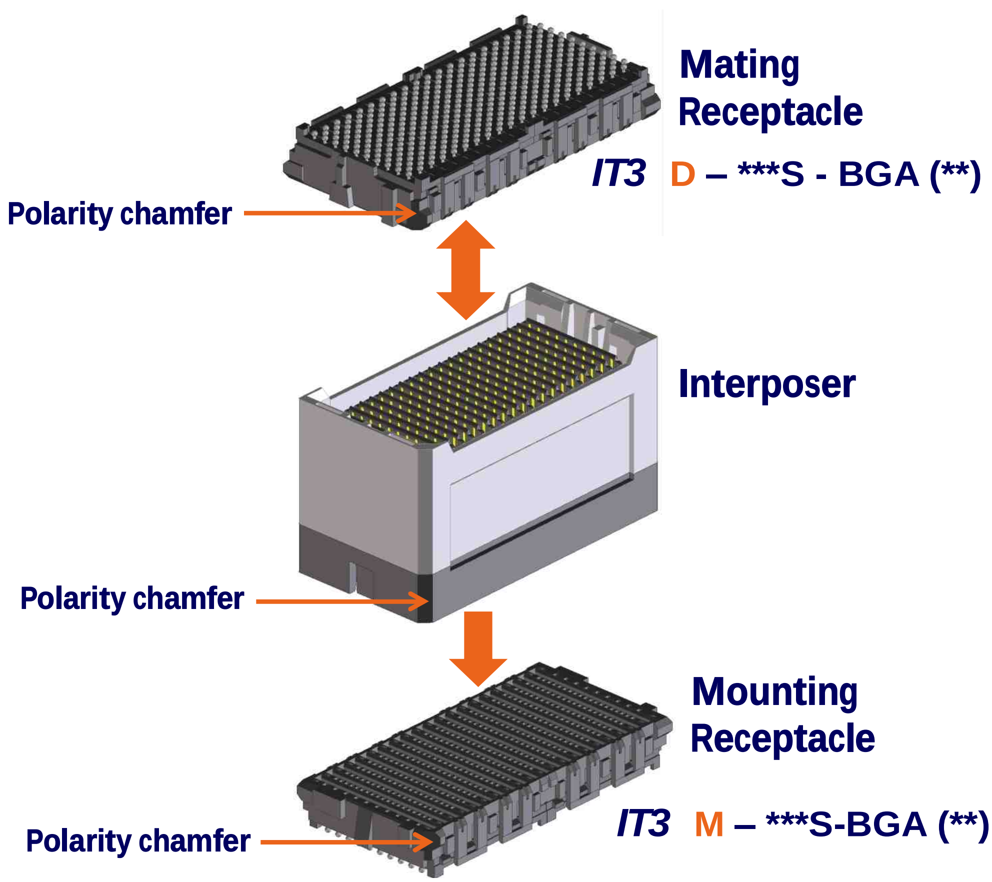
The Hirose IT3 connector's footprint is a staggered area array that allows space for easy via placement and signal routing between pads. Each row of I/O's alternates signal and ground interconnections. It is mounted to the board as a lightweight receptacle, and an interposer is used to connect to parallel PWBs at multiple different height options. Spacers must be used in conjunction with the interposers to help reinforce the structure of the final multi-PWB assembly.

This section of the Design Note discusses multi-connector systems, clearance between connectors, interposer direction, and alignment tolerances.

5.1 Footprint

5.1.1 Polarity

Each receptacle and interposer has **one corner chamfered** to insure proper orientation during assembly and installation. The corner with the **chamfer is nearest to pin A1**.



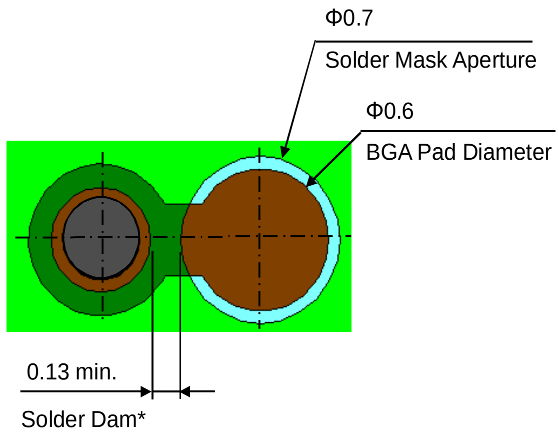
Annotation

For **visual inspection** purposes, **"Pin 1"** should be denoted on the silkscreen of the PWB by a **specific marking** (e.g. asterisk or other accepted symbol) near the A1 contact location and chamfer.

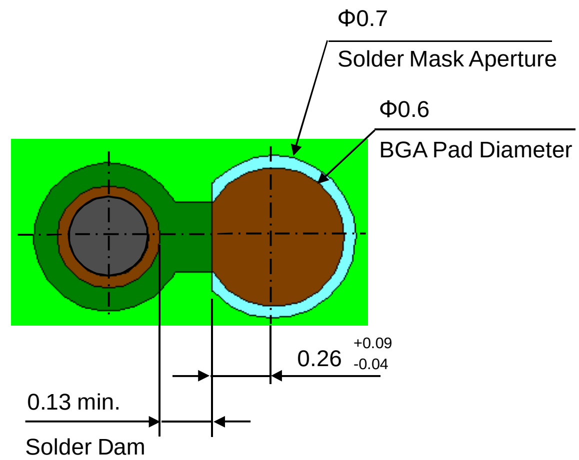
5.1.2 Pad Specification

0.6mm diameter Non-Solder Mask Defined (NSMD), also known as *copper defined* or *metal defined,* pads are recommended. Recommended sizes and clearances are shown below:

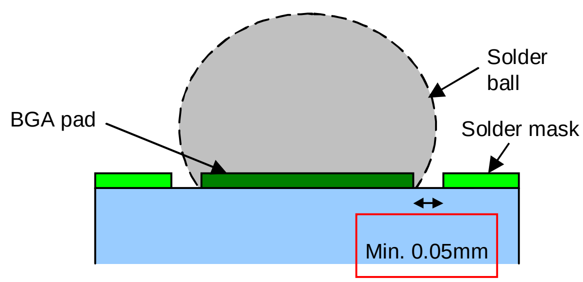
HIROSE
Recommended Pad Design



Acceptable Pad Design



* All dimensions shown are in mm



Cross Section of Pad and Solder ball

- Keep minimum clearance 0.05mm between BGA pad and solder mask to achieve “copper defined BGA pad”.
- BGA pad finish: OSP (Organic Solderability Preservative) or HASL (Hot Air Solder Leveler).
- The drill diameter of 0.34mm is for reference only. Use the proper aspect ratio of board thickness to via drill diameter for each PCB fabricator.

Through-via sizes will **depend on PWB thickness** and fabricator's capabilities. Vias should be placed far enough from the pad to ensure a **minimum** solder **dam width of 0.13mm**. **Circular openings** in the solder mask are **preferred,** but **D-shape openings** are **acceptable** if the minimum spacing requirement is met.

PWB pad finish is typically **Organic Solderability Preservative (OSP)** or **Hot Air Solder Level (HASL)**, but the component can also be used with Electroless Nickel-Immersion Gold (ENIG), Immersion Silver and Immersion Tin.

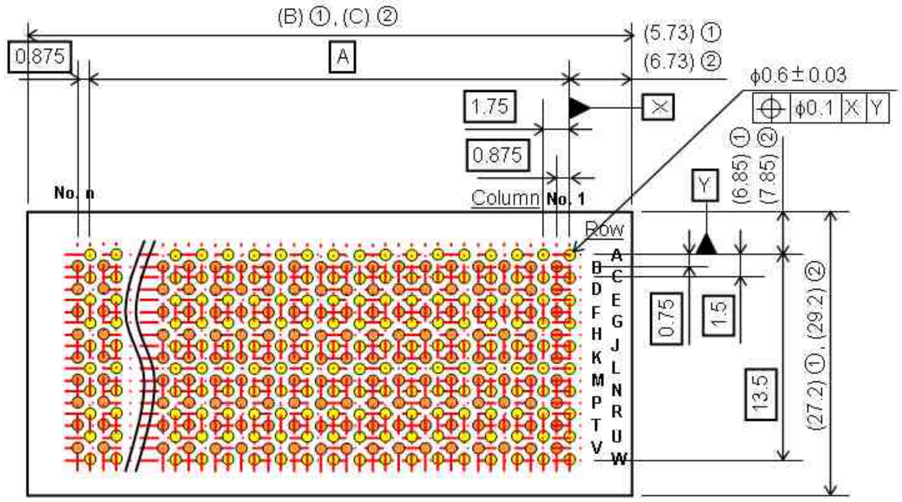
The **stencil apertures** should be **0.54mm circles**, concentric with the copper pads. This represents a 10% reduction from the diameter of the pad to compensate for typical variations in the assembly process.

The specified clearance, or **solder mask relief**, from the copper feature **is 0.05mm**.

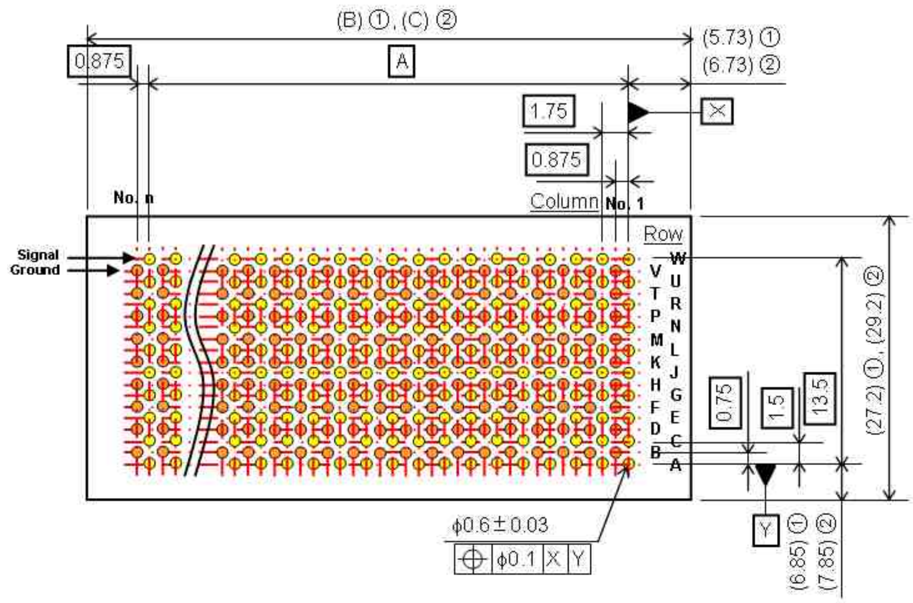
Precaution

Verify fabricator capability. **Solder mask registration** must be accurate to at least **0.05mm**. PWB fabricator's registration capability should be verified. Depending on the thickness of PWB, fabricator's **aspect ratio** capabilities **for through vias** should also be verified.

5.1.3 Component Footprint and Contact Assignment



Mounting Receptacle – *IT3-M*



Mating Receptacle – *IT3-D*

① Minimum clearance for all devices
② Minimum clearance for sensitive devices

Signal Pad
Ground Pad

*** All dimensions shown are in mm.**

Dimension (mm)	100	200	300
A	15.75	33.25	50.75
B	28.10	45.60	63.10
C	30.10	47.60	65.10

5.1.4 Contact Assignment

Figure 1 shows the side view of the IT3 connector. Figures 2and 3 show the pin assignments on the PCB. Odd-numbered columns are signals and the even-numbered columns are grounds.

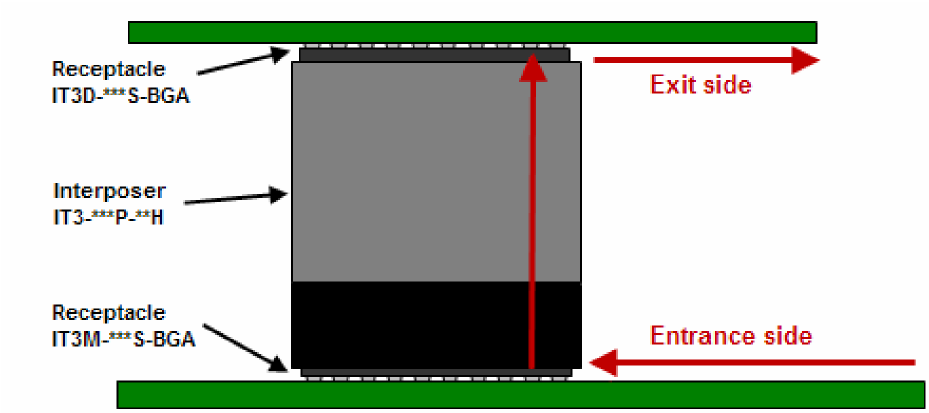


Figure 1 IT3 connector side view

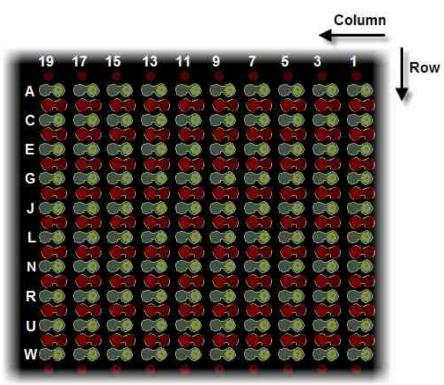


Figure 2 BGA pin-out on Motherboard PCB

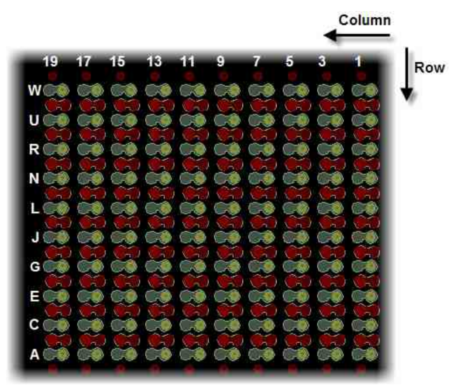


Figure 3 BGA pin-out on Daughterboard PCB

5.1.5 Routing Suggestions / Examples

The traces are routed in the column direction, avoiding going over the anti-pad. To avoid intra-pair skews, the trace lengths are matched. All trace bends are at 45-degree angles. Routing on adjacent dual strip line layers is not recommended and non-functional signal pads should be removed. Figures 4, 5 and 6 show examples of BGA pad layout, single-ended trace and differential trace routing on the PCB.

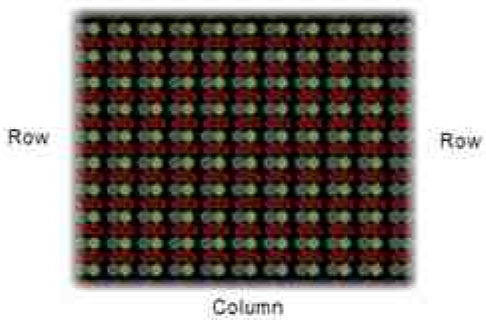


Figure 4 BGA Pad Layout on PCB

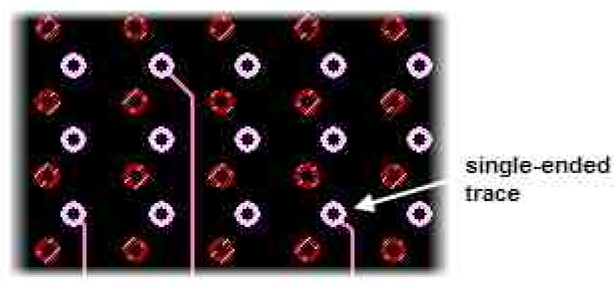


Figure 5 BGA Pad Layout on PCB

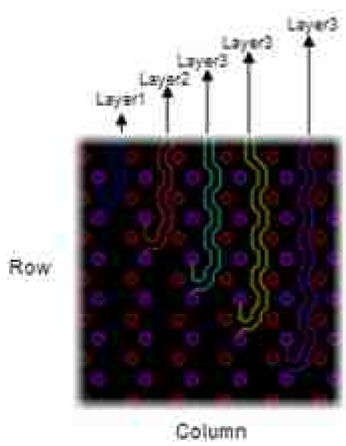


Figure 6-a Differential Routing

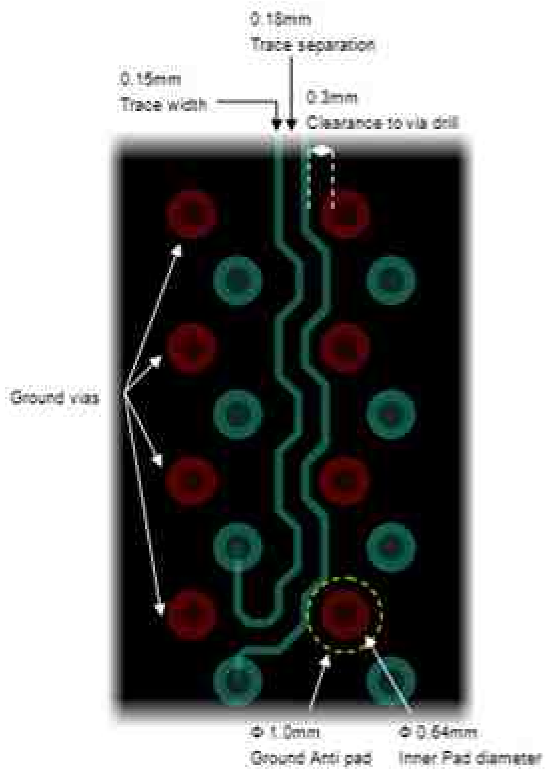


Figure 6-b Details of differential routing design

As shown in Figure 7, a minimum of three routing layers must be used on the PCB. Also, additional columns and rows of ground vias are added beyond row A, row W, and column 19 (for 100 pos.) to ensure that each signal via on the PCB is surrounded by four ground vias.

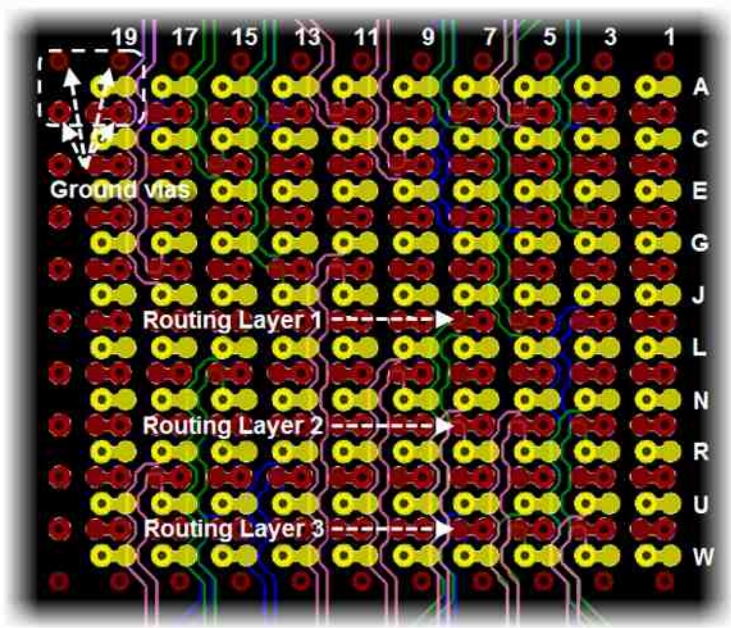


Figure 7 IT5 connector pin-out

A suggested trace routing example for differential signals is shown in Figure 11, with the stack up from Figure 12. The width and spacing of the differential signal traces must satisfy the following criteria:

$$2*W + S < CP - D - 2*C_{dt}$$

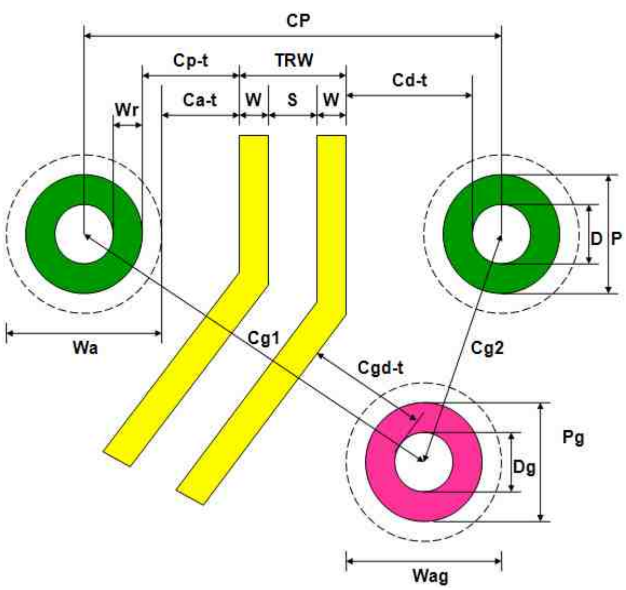
$$2*W + S < CP - W_a$$

$$2*W + S < C_{g1} - \frac{D_g}{2} - C_{gdt} - \frac{D}{2} - C_{dt}$$

$$2*W + S < C_{g1} - \frac{W_a}{2} - \frac{W_{ag}}{2}$$

For a 120 mil board, the signal and ground via sizes, and clearance from via drill are fixed. Therefore, only the trace width and spacing are adjustable.

Single ended traces can be routed anywhere within the limits of the total routing width (TRW) for the differential signals.



		Reference Distance	Min *
Column Pitch	CP	1750 µm	---
Trace	W	4 mil	---
Spacing	S	8 mil	---
Pad	P	22 mil	---
Antipad	Wa	40 mil	---
Drill (10:1 ratio)	D	12 mil	12 mil
Annular Ring	Wr	5 mil	---
Total Routing Width	TRW	16 mil	---
Clearance Antipad-Trace	Ca-t	6 mil	---
Clearance Pad - Trace	Cp-t	15 mil	---
Clearance Drill - Trace	Cd-t	20 mil	20 mil
Antipad (ground via)	Wag	40 mil	---
Pad (ground via)	Pg	22 mil	---
Drill (ground via)	Dg	12 mil	12 mil
Clearance Drill (ground via) - Trace	Cgd-t	10 mil	10 mil
Ground to signal via 1	Cg1	1436 µm	---
Ground to signal via 2	Cg2	916 µm	---

* minimum dimension due to process limitations

Figure 11 Trace routing example

Layer No.			Mil
		Solder mask	0.5
1	TOP		2.84
		Pre-preg	4.5
2	Ground		0.7
		Core	3
3	Sig 1		0.7
		Pre-preg	3.5
4	Sig 2		0.7
		Core	3
5	Ground		0.7
		Pre-preg	3.5
6	Ground		0.7
		Core	3
7	Sig 3		0.7
		Pre-preg	3.5
8	Sig 4		0.7
		Core	3
9	Ground		0.7
		Pre-preg	3.5
10	Ground		0.7
		Core	3
11	Sig 5		0.7
		Pre-preg	3.5
12	Sig 6		0.7
		Core	3
13	Ground		0.7
		Pre-preg	3.5
14	Ground		0.7
		Core	3
15	Sig 7		0.7
		Pre-preg	3.5

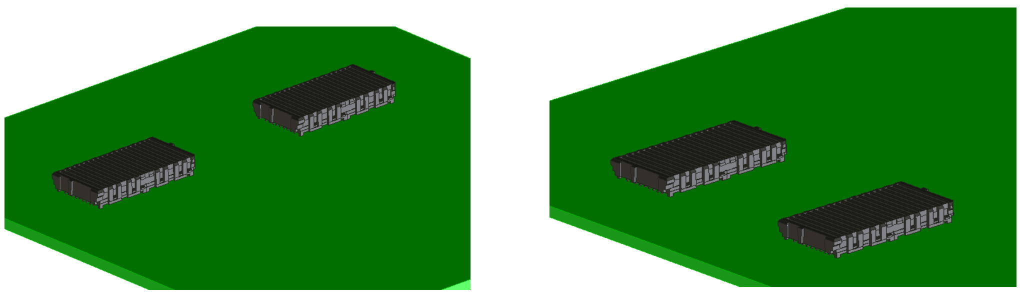
Layer No.			Mil
16	Sig 8		0.7
		Core	3
17	Ground		0.7
		Pre-preg	3.5
18	Ground		0.7
		Core	3
19	Sig 9		0.7
		Pre-preg	3.5
20	Sig10		0.7
		Core	3
21	Ground		0.7
		Pre-preg	3.5
22	Ground		0.7
		Core	3
23	Sig11		0.7
		Pre-preg	3.5
24	Sig12		0.7
		Core	3
25	Ground		0.7
		Pre-preg	3.5
26	Ground		0.7
		Core	3
27	Sig13		0.7
		Pre-preg	3.5
28	Sig14		0.7
		Core	3
29	Ground		0.7
		Pre-preg	4.5
30	BOTTOM		2.84
		Solder mask	0.5
	Total thickness (mil)		121.78

Figure 12 PCB stack up example

5.2 Multi-Connector Systems

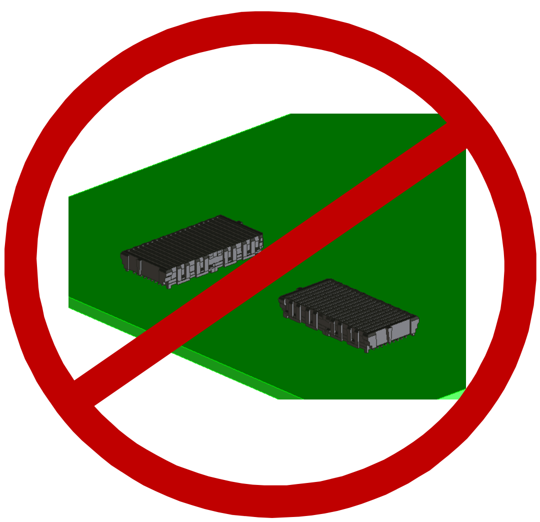
*The **IT3** connectors can be used singularly or in combination with other **IT3** connectors.*

If multiple connectors are used on the same PWB, they must be oriented in the same direction, as shown below:



Correct Orientations

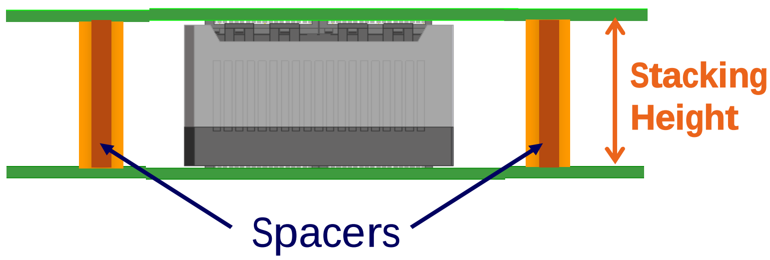
It is not recommended to mix orientations:



Do not mix orientations

5.3 Spacers

Spacers are required to support the PWB's and protect the BGA solder joints.



Suggested spacer style is shown below:

Spacer, male-male, M3 thread

The recommended spacer height corresponds to the interposer stacking height as shown in the chart below:

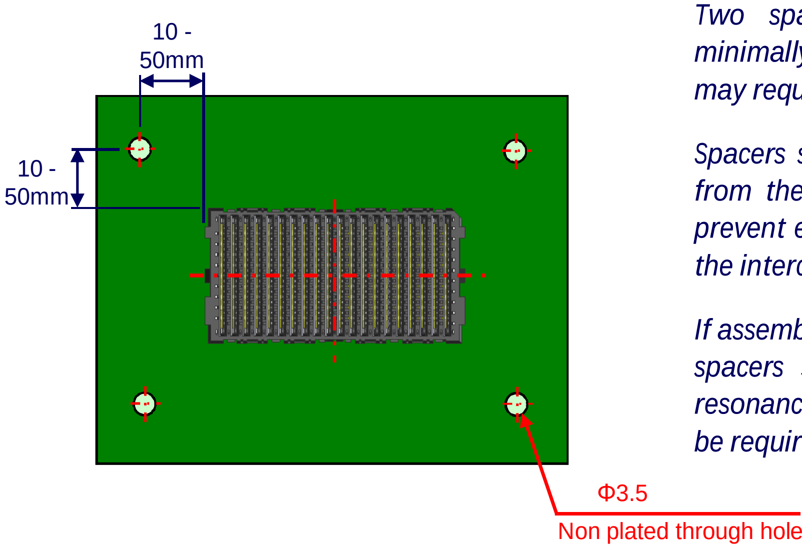
Stacking Height	Recommended Specer Height
14 mm	14 +/-0.127 mm
15 mm	15 +/-0.127 mm
17 mm	17 +/-0.127 mm
18 mm	18 +/-0.127 mm
20 mm	20 +/-0.127 mm
22 mm	22 +/-0.127 mm
25 mm	25 +/-0.127 mm
26 mm	26 +/-0.127 mm
28 mm	28 +/-0.127 mm
30 mm	30 +/-0.127 mm
32 mm	32 +/-0.127 mm
35 mm	35 +/-0.127 mm
38 mm	38 +/-0.127 mm
40 mm	40 +/-0.127 mm

5.3.1 Spacer Location

Two spacers located diagonally are minimally required. Some applications may require four spacers.

Spacers should be located 10 – 50 mm from the corners of the receptacles to prevent excessive mechanical loading on the interconnections.

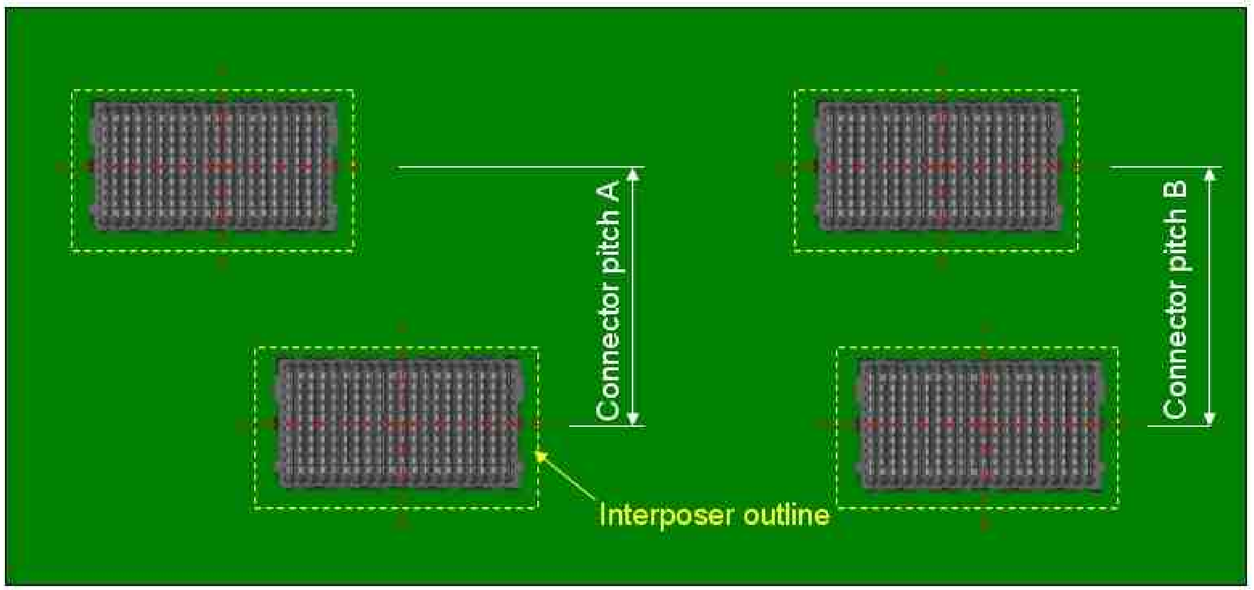
If assembly will be subjected to vibration, spacers should be located to prevent resonance, and additional spacers may be required.



Recommended Spacer Location

5.4 Clearance between Connectors and Other Components and PCB Edge

Parallel Mounting



Not in scale

(A) If **overlap distance is less than half** the length of the connector:

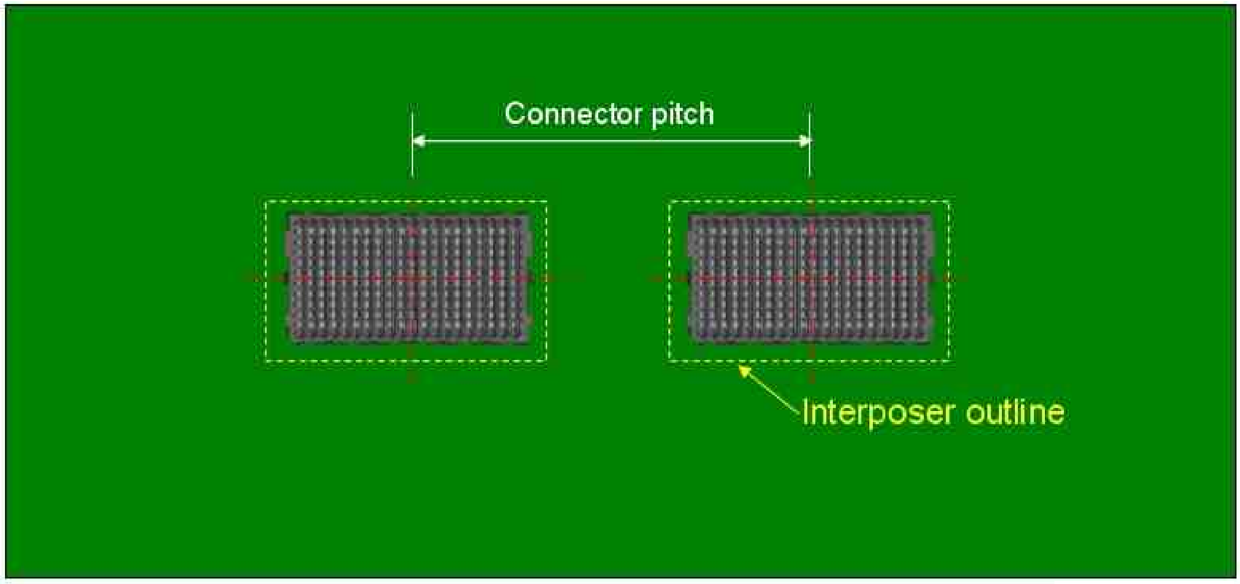
Socket Combinations	Connector Pitch A (Max)	Connector Pitch A (Min)
All combinations	24.10 mm	209.20 mm

(B) If **overlap distance is more than half** the length of the connector:

Socket Combinations	Connector Pitch B (Max)	Connector Pitch B (Min)
All combinations	31.00	209.20

Suggested clearances are based on accessibility to grip interposer for purposes of disassembly and field replacement.

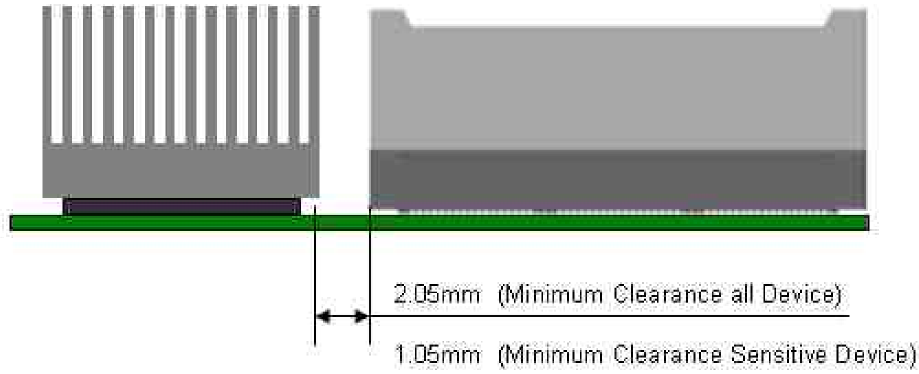
Tandem Mounting

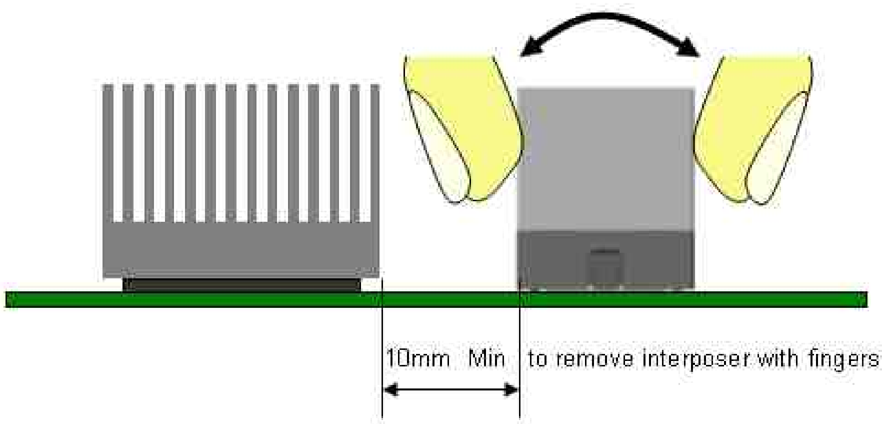


Not in scale

Socket Combinations	Connector Minimum Pitch (mm)	Connector Maximum Pitch (mm)
IT3-100pos + IT3-100pos	26.05	211.00
IT3-100pos + IT3-200 pos	34.80	219.75
IT3-100pos + IT3-300 pos	43.55	228.50
IT3-200pos + IT3-200 pos	43.55	228.50
IT3-200pos + IT3-300 pos	52.30	237.25
IT3-300pos + IT3-300 pos	61.05	246.00

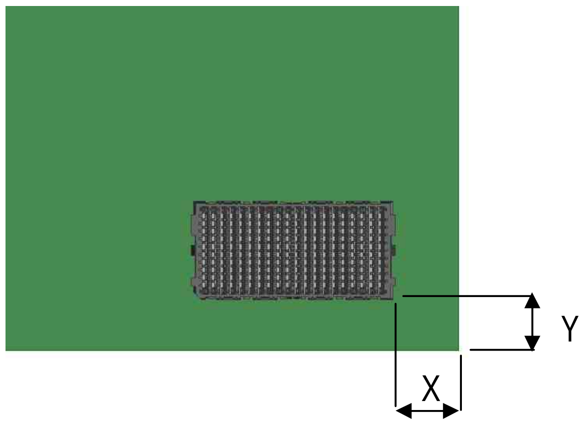
Clearances between a connector and other components





Clearance between the receptacle and PCB edges

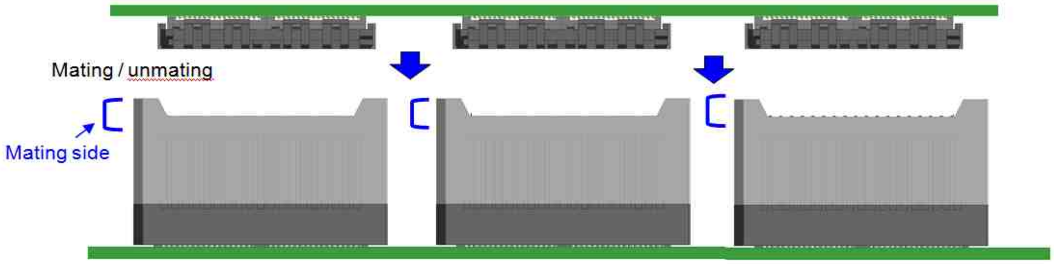
Please communicate CEM regarding the clearance especially when requiring the top side reflow.



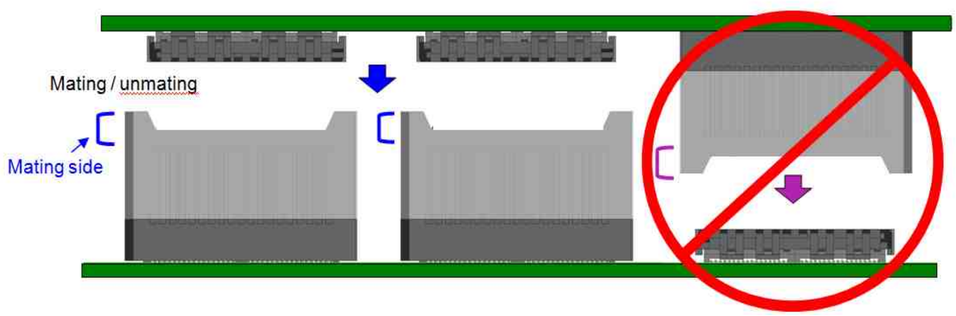
5.5 Interposer Direction

Do not mix mating and mounting receptacles on the same PWB.

All interposers must engage in the same direction, as shown below:



Correct Method – all connectors mate in same direction

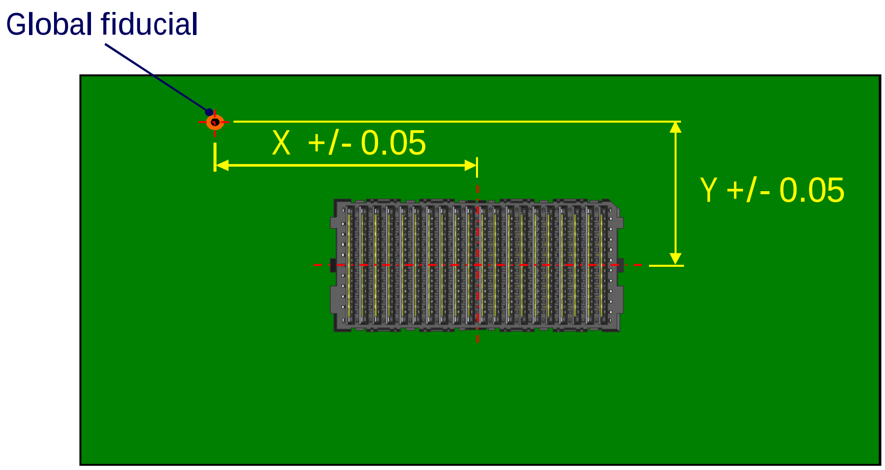


Incorrect Method – connectors mate in different directions

5.6 Alignment Tolerances

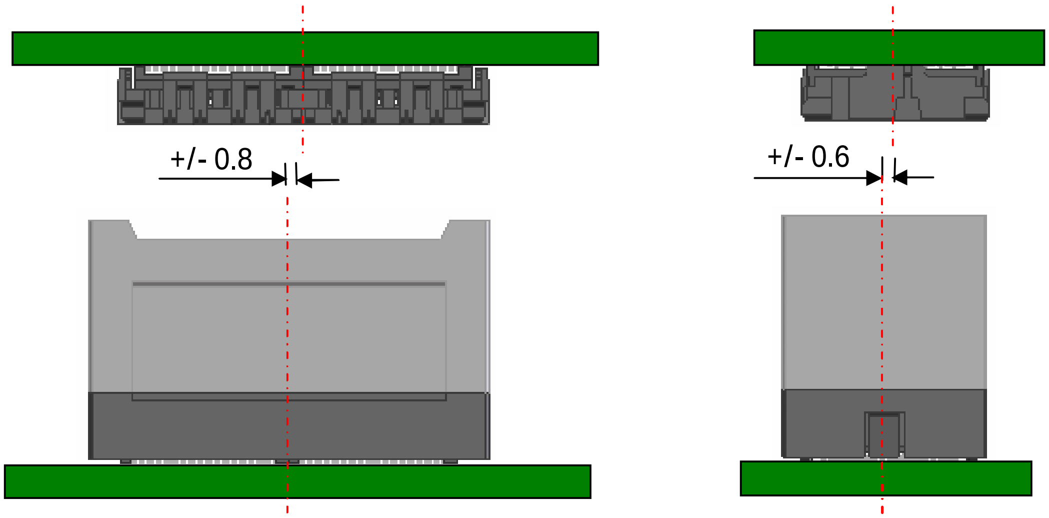
5.6.1 Mounting Tolerances

Mounting tolerances of ± 0.05mm are required for robust SMT assembly and to ensure proper mating fits in cases of multiple connectors:



*All dimensions shown are in mm.

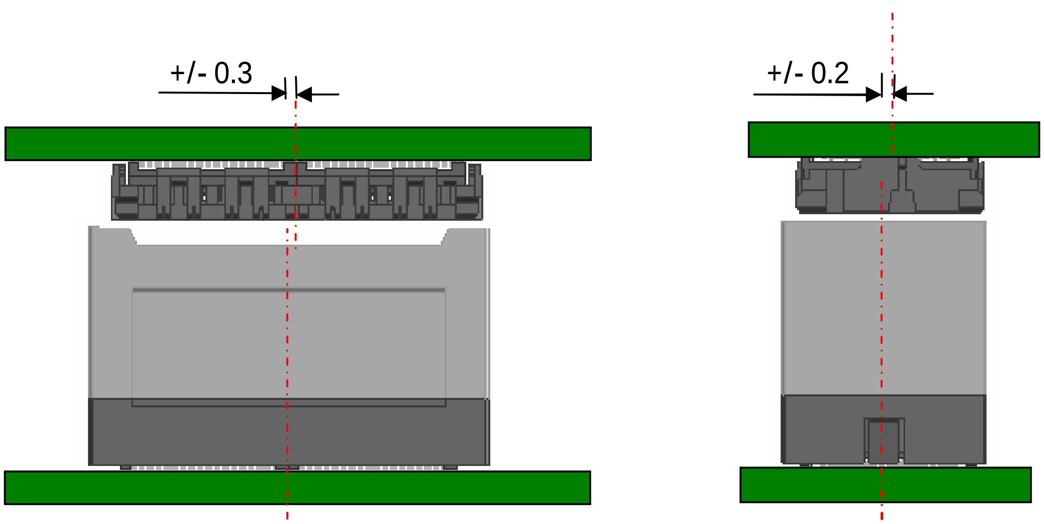
5.6.2 Mating Self Alignment



X-direction Y-direction

5.6.3 Mating Tolerances

Due to its 3-piece design, the IT3 connector system can accept mating tolerances of up to ±0.3mm tolerance in the X-axis and up to ±0.2mm in the Y-axis.



X-direction Y-direction

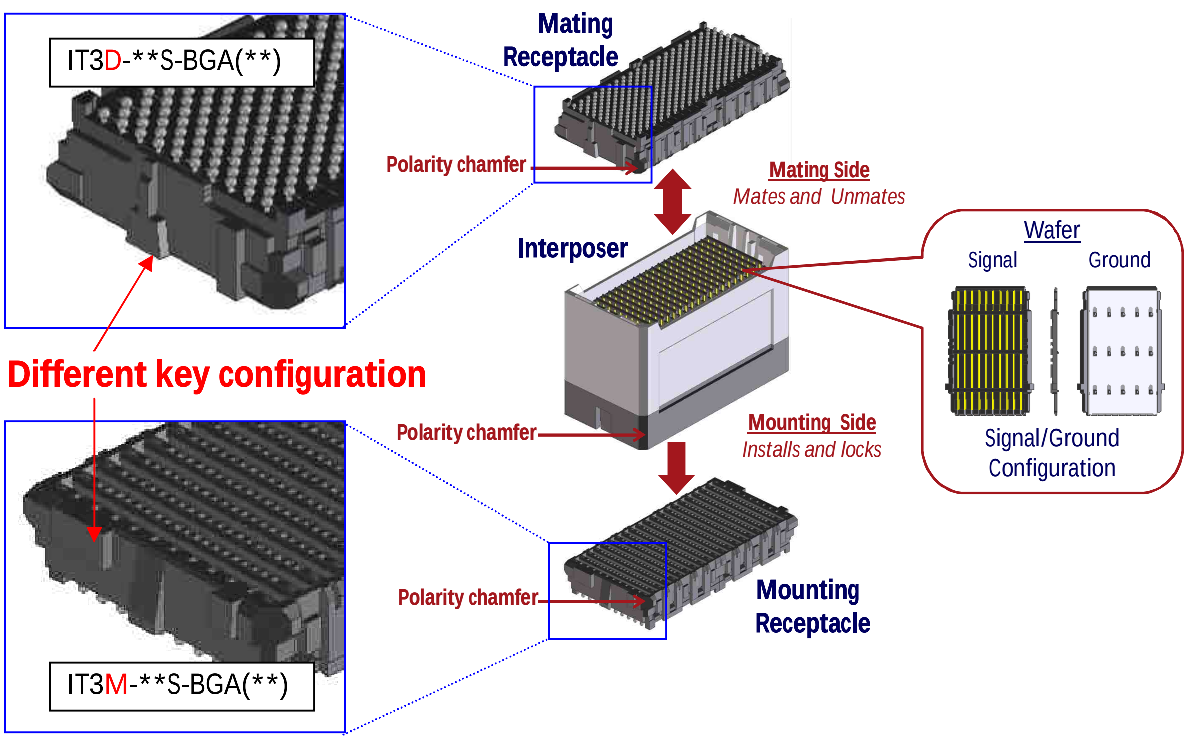
* All dimensions shown are in mm

Section 6 Assembly Process

This section of the Design Note discusses summarized IT3 assembly process and interposer installation / removal. As for details, please refer to Assembly note "ETAD-F0457"

6.1 Overall Assembly Process

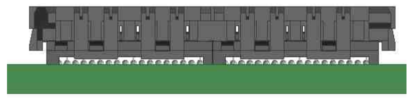
6.1.1 Difference between Mating Receptacle and Mounting Receptacle



6.1.2 Assembly Process

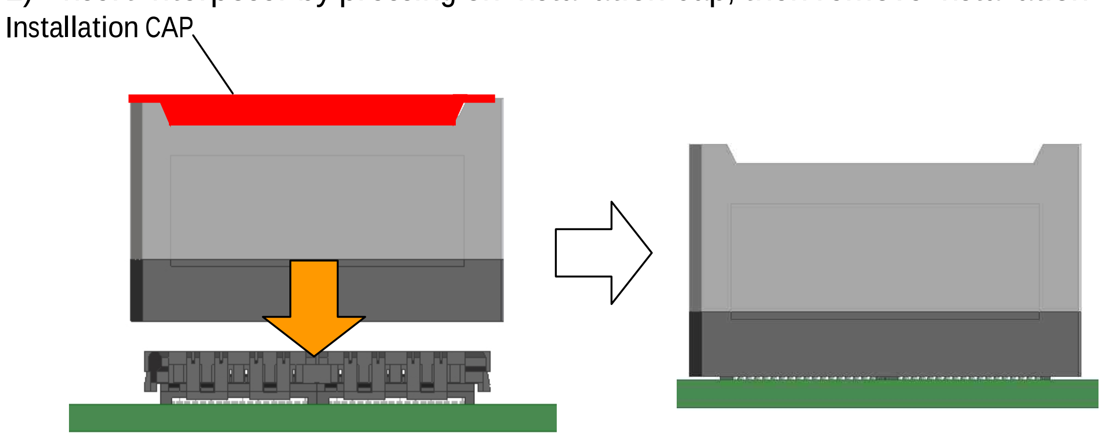
IT3 Assembly Process

1) Reflow Mounting Receptacle (IT3M) on PCB



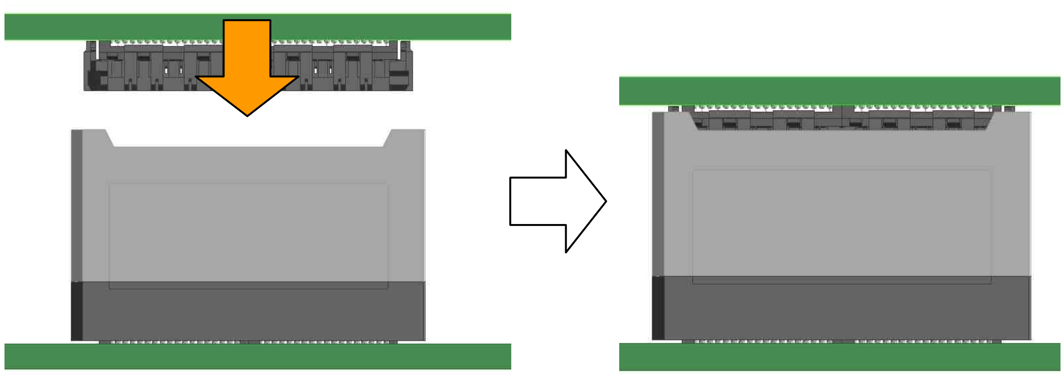
Caution: No Reflow with Interposer

2) Insert Interposer by pressing on Installation Cap, then remove Installation Cap



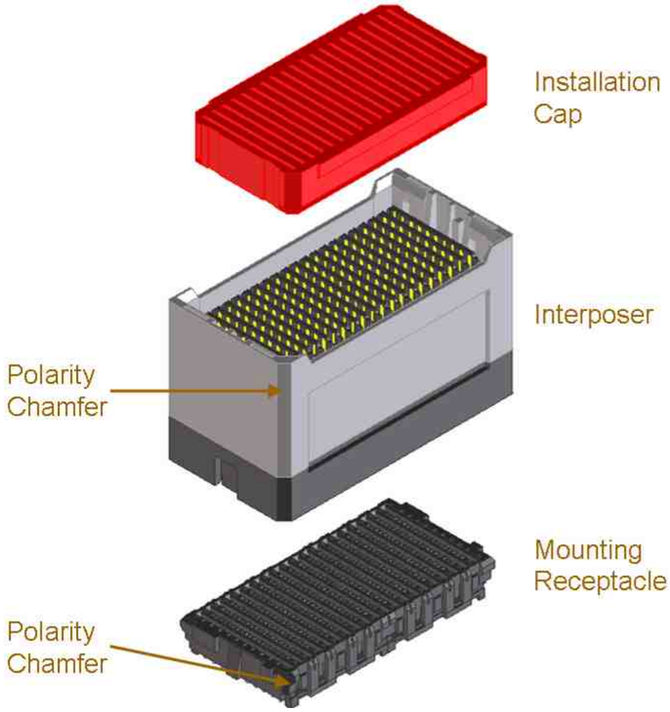
Caution: No touch and push wafers in Interposer

3) Insert Mating Receptacle (IT3D)



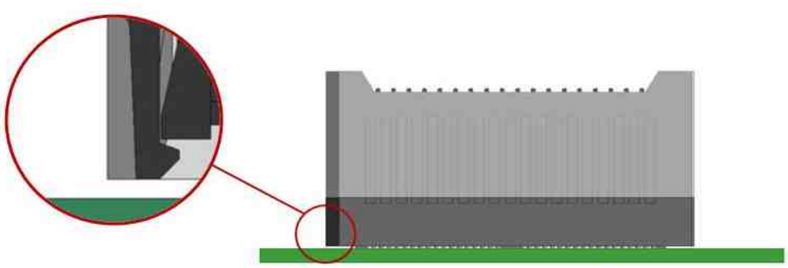
6.2 Interposer Installation

The interposer snaps on to the mounting receptacle as shown below:

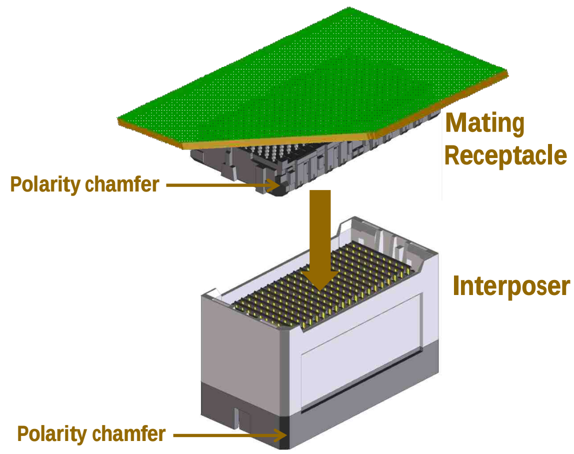


The snap fit is achieved by a locking latch on each end of the interposer:

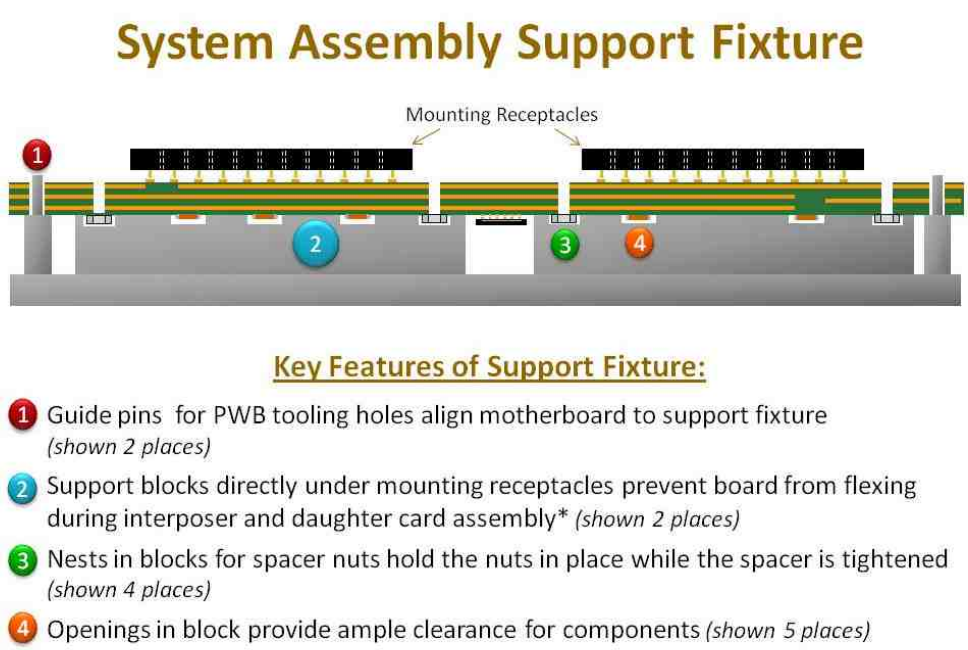
Locking Latch



The spacers are installed (not shown) and the mating receptacle is aligned with the interposer and pressed on as shown below:



It is very important to provide good underside board support when installing the interposers. A simple tooling plate can be fabricated to support the PWB and prevent it from flexing when the interposers are installed:



* For more information on PWB support and allowable deflections, reference IPC-JEDEC 9704, *Printed Wiring Board Strain Gage Test Guideline.*

The following maximum angles should not be exceeded during manual installation of the daughter card as shown below:

- o Longitudinal: 3°
- o Lateral: 10°

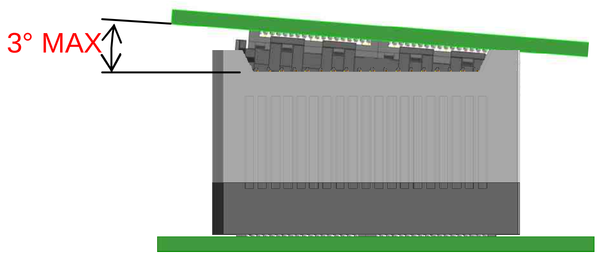


Fig.1 Longitudinal

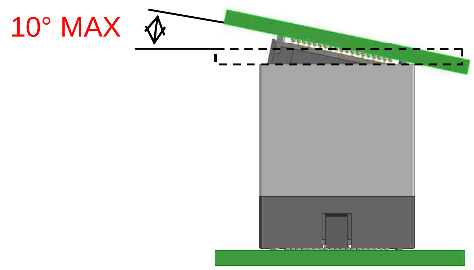
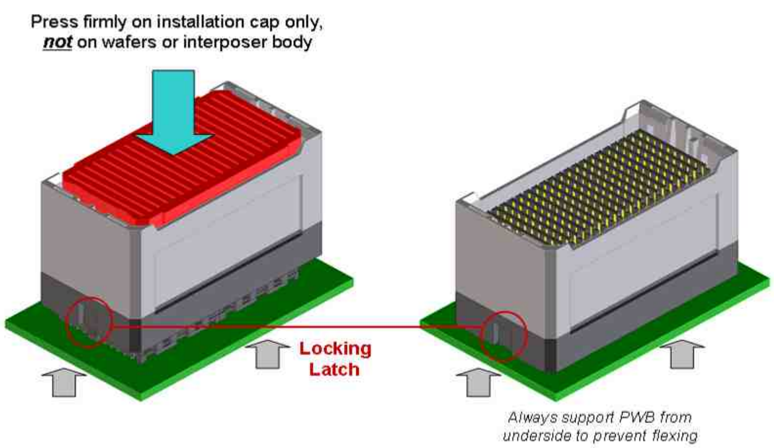


Fig.2 Lateral

Hirose recommends consideration of the above allowable angles and the orientation of the daughter card for manual assembly during the design process. Hirose also recommends the use of spacers as mentioned on Chapter 5.3 so the tip of the spacers will be fulcrum points that allow operators to accomplish daughter card assembly with small angles.

Position interposer directly over mounting receptacle, aligning the polarity chamfers. If positioned properly, the interposer should slide easily onto the mounting receptacle. The side with horizontal grooves should face up. Place the installation cap into the interposer, and push the interposer down through the installation cap to engage the locking latches:

Manual Installation

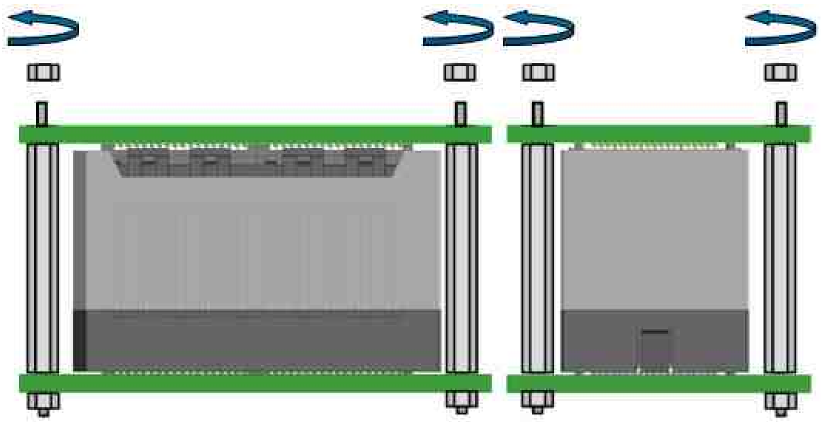


After the interposer is mounted, install spacers onto motherboard (not shown).

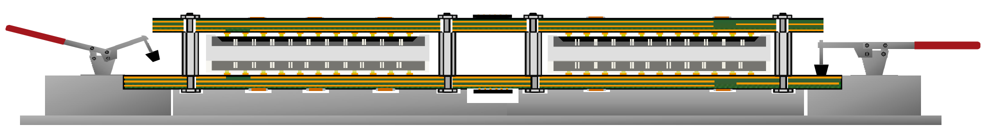
6.3 Overall Disassembly Process

The Hirose **IT3** three-piece connector system can be disassembled if a mother board or daughter card requires replacement. Both the mating receptacle and the interposer are removable. When removing a card or a connector component, the circuit boards should be handled with great care to prevent damage to them. Failure to properly remove the circuit boards or interposers can result in permanent damage to the circuit assemblies.

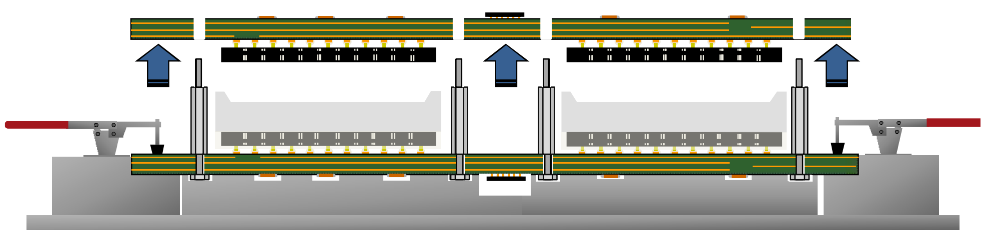
To remove a daughter card, first remove the nuts from the reinforcing spacers.



It is very important to prevent excessive flexing of the circuit assemblies during disassembly operations. To minimize flexing of the mother board, a simple tooling plate is suggested.



The tooling plate has clamps to stabilize the mother board while the daughter card (and possibly the interposer) is removed. The daughter card should be lifted straight up off the interposers.



To minimize unnecessary flexing of the daughter card, the removal forces should be applied as close to the interposer as possible without contacting any components. On densely populated assemblies, the edges may be the only open area that can be grasped.

The following maximum angles should not be exceeded during disassembly of the daughter card as shown below:

- Longitudinal: 3°
- Lateral: 10°

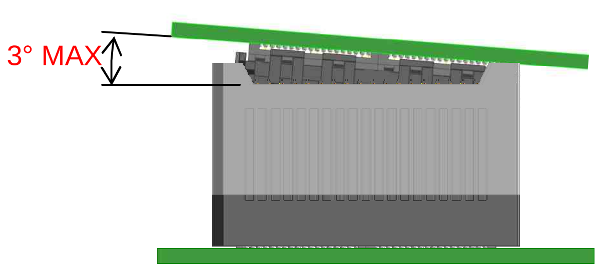


Fig.1 Longitudinal

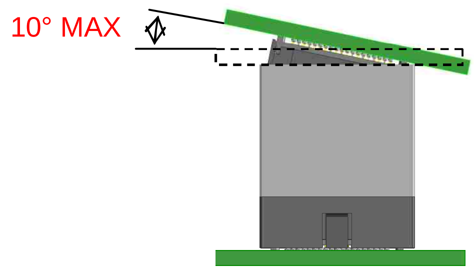


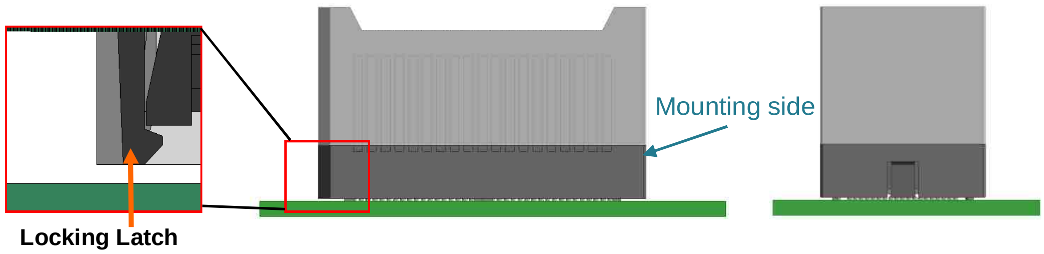
Fig.2 Lateral

Hirose recommends consideration of the above allowable angles and the orientation of the daughter card for manual disassembly during the design process. Hirose also recommends the use of spacers as mentioned on Chapter 5.3 so the tip of the spacers will be fulcrum points that will allow operators to accomplish daughter card disassembly with small angles.

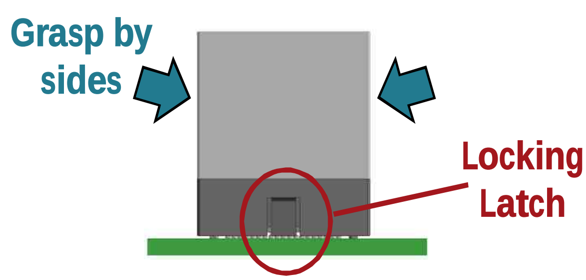
6.4 Interposer removal

The interposer is secured onto the mounting receptacle with a snap fit tab, as shown below:

The removal shall be 5 times max.

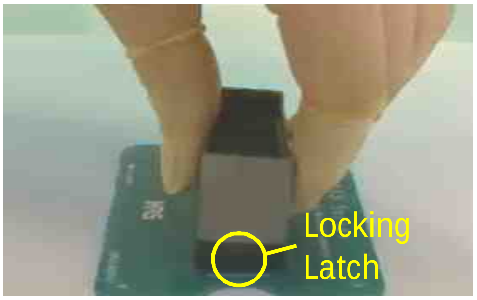


For removal, interposer should be grasped by the sides shown. These sides of the interposer do not have locking latches.

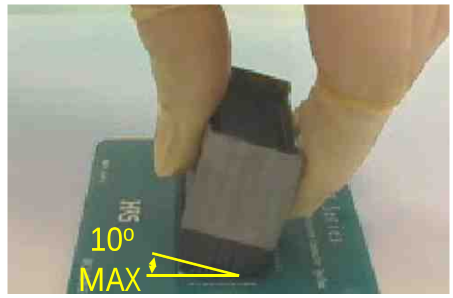


Interposer Removal by Hand

1) Hold the Interposer Assembly on the walls without locking latches.

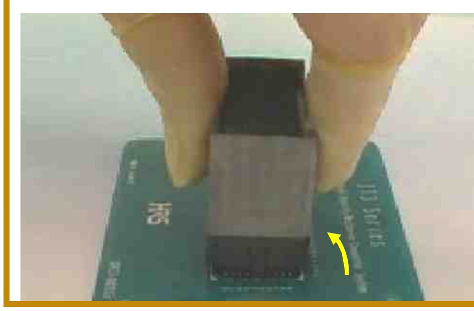


2) Gently rotate one side of the Interposer Assembly laterally 10° maximum

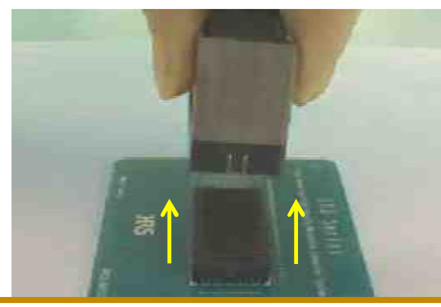


Caution: do not rotate more than 10 degrees

3) While gently rotating, pull up on other side of the Interposer Assembly



4) The Interposer Assembly is removed, and the Mounting Receptacle is ready to accept another Interposer Assembly.



An interposer removal tool is also available. **This tool is not an interposer installation cap, so please do not use it to install an interposer.** Doing so may damage an interposer.

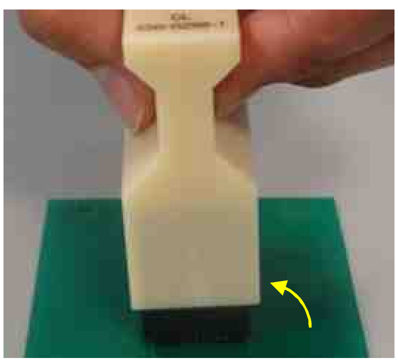
Interposer Removal with Tool

1) Cover the Interposer Assembly with the interposer removal tool

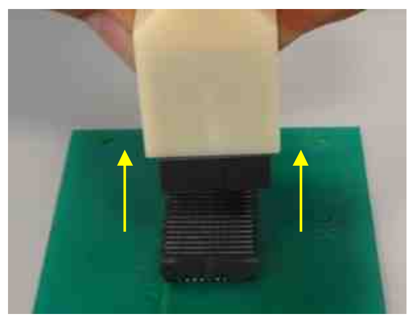
2) Gently rotate one side of the Interposer Assembly laterally 10° maximum using the tool

Caution: do not rotate more than 10 degrees

3) While gently rotating, pull up on other side of the tool



4) The Interposer Assembly is removed, as it is inside the tool



Precaution

Visually inspect the interposer before reinstalling it. Discard if it shows any sign of damage or wear. Do not subject the interposer assembly to more than five removal-reinstallation cycles, even if it appears unaffected.

Section 7 Technical Document Library

Following data and documents are available.

7.1 Technical Data

No	Item	Format	File name (Ex.)
1	Simplified 3D model	STEP (SAT &IGES are also available)	IT3M-300S-BGA.stp
2	Footprint data	Allegro	IT3M-300S-BGA.brd
3	Spice models	Spice	IT3-**H.sp
4	Touchstone model	Touchstone	IT3-300-**H.s60p

7.2 Technical Document

No	Item	Format	File name (Ex.) or Document number
1	2D drawing	PDF	IT3M-300S-BGA.pdf
2	Spec sheets	PDF	IT3M-300S-BGA.pdf
3	Contact reliability report	PDF	TR0636E-10018
4	Eutectic thermal cycling test report	PDF	TR0636E-10026
5	Lead free thermal cycling test report	PDF	TR0636E-20128
6	Temperature rise report	PDF	TR0636E-20041
7	SI report	PDF	IT3-**H.pdf
8	Assembly note	PDF	ETAD-F0457
9	Design note	PDF	ETAD-F0347
10	Customer demo board test report	PDF	IT3_demo_board_v2.pdf
11	Characterization board test report	PDF	IT3_Characterization_Board_v09.pdf

HIROSE ELECTRIC (U.S.A.), INC.
High Speed Interconnects
20400 Stevens Creek Blvd., Suite 250, Cupertino, CA 95014, U.S.A.
www.hiroseusa.com

email: IT3@hirose.com