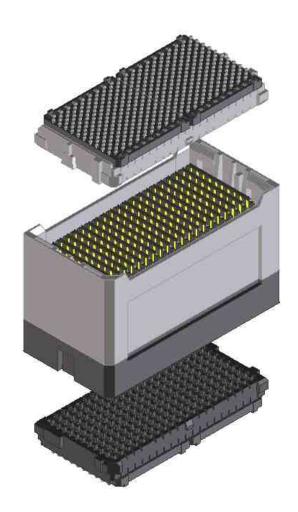
Hirose *IT5* ™ Connector System Design Notes





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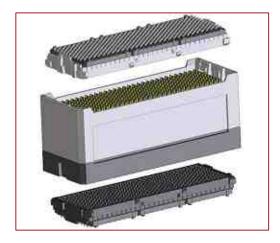


Revision No.	Description (Major changes)	Date
0.9	Preliminary release	August 8, 2011
0.95	Revised Sections 2 and 4	April 30, 2012
1.00	Revised Sections 2, 5 and 6	January 7, 2013
1.01	Revised Section 5	March 26, 2013



Section 1 Introduction

The Hirose **IT5** connector system is a three-piece mezzanine connector. Process-friendly BGA receptacles are assembled onto PWBs, and separate, configurable interposers complete the connections between circuit boards. 100, 200 and 300 signal models with lead-free alloys are available.



Hirose IT5 connector assembly

This section of the Design Note discusses purpose, scope, and application and interpretation.

1.1 Purpose

This technical bulletin is intended to provide basic information and product features of the Hirose *IT5* BGA connector system. By providing this information, Hirose believes it can help its customers to speed product development, improve quality and reliability, and limit overall system costs.



1.2 Scope

This guideline provides information useful for applications using the *IT5* BGA connector system. It provides information pertaining to:

- a) General Information
- b) Operating Characteristics
- c) Signal Integrity
- d) PWB design Information
- e) Assembly process

This document will be updated by Hirose as required to reflect current technologies and manufacturing capabilities.

1.3 Application and Interpretation

This technical bulletin is intended to offer only general guidance and design concepts to customers. It does not limit customer designs nor guarantee results under all situations. Development of actual designs is the responsibility of each customer. Customers should consult with Hirose regarding their specific application, when, or if, any questions arise relating to these guidelines. Use of this technical bulletin is at customer's sole risk. This bulletin is provided "AS IS" and without warranty of any kind and Hirose EXPRESSLY DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. HIROSE DOES NOT WARRANT THAT THE GUIDELINES CONTAINED IN THIS BULLETIN WILL MEET ANY CUSTOMER'S REQUIREMENTS. FURTHERMORE, HIROSE DOES NOT WARRANT OR MAKE ANY REPRESENTATIONS REGARDING THE USE OR THE RESULTS OF THE USE OF INFORMATION CONTAINED IN THIS BULLETIN IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. UNDER NO CIRCUMSTANCE SHALL HIROSE OR ITS DIRECTORS, OFFICERS, EMPLOYEES OR AGENTS BE LIABLE FOR ANY INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES (INCLUDING DAMAGES FOR LOSS OF BUSINESS, LOSS OF PROFITS, BUSINESS INTERRUPTION, LOSS OF BUSINESS INFORMATION AND THE LIKE) ARISING OUT OF THE USE OF THE INFORMATION CONTAINED IN THIS BULLETIN.

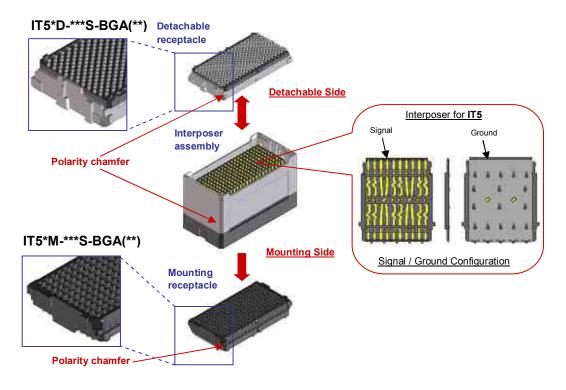


Section 2 General Information

Hirose's **IT5** connector system is designed to provide modular high-speed differential, single-ended and power connections between two parallel boards. The interconnection to the PWBs utilizes process-friendly Ball Grid Array receptacles, while the stacking height of 18 to 40mm is set by an impedance-controlled interposer that is added at the system level.

The **IT5** connector system consists of two receptacles and one interposer. The receptacles have low profiles and open bodies. The BGA balls are mounted on compliant pins and are set on a staggered grid of 1.5 and 1.75 mm pitch. Both the detachable and mounting receptacles' footprints are compatible with popular mezzanine connectors. Receptacles are available in lead-free configurations, and can be used in no-clean or water-wash assembly processes.

The interposer is an assembly consisting of individual wafers, each carrying 10 signal and 11 ground connections. The interposer is mounted to the receptacles and locked in with mechanical latches to create highly reliable and stable mechanical and electrical connections.



This section of the Design Note discusses component weights, part number designation, and general dimensions.



2.1 Stacking Height Variations

2.1.1 IT5 stacking height variations

The M side and D side receptacle combination and IT5 interposer wafer height will achieve an 18mm-40mm stacking height.

Rece	IT5 Interposer wafer							
M side (Mounting side)	D side (Detachable side)	18H	22H	25H	28H	32H	35H	38H
IT5M	IT5D	18mm	22mm	25mm	28mm	32mm	35mm	38mm
ІТ5НМ	IT5D	19mm	23mm	26mm	29mm	33mm	36mm	39mm
IT5M	IT5HD	19mm	23mm	26mm	29mm	33mm	36mm	39mm
ІТ5НМ	IT5HD	20mm	24mm	27mm	30mm	34mm	37mm	40mm



2.2 Component Weights

2.2.1 IT5 Weight by assembly process

	As	Assembly Process using IT5M and IT5D Receptacles							
	(I ^r after	ceptac T5M/D cap / ta emove	ape is	after	otacle (Interpo nstalle	oser is	two (IT5 a	rposer Recept 5M & 17 fter fin ssemb	racles (T5D) al
Stacking				Cont	tact po	sition			
Height	100	200	300	100	200	300	100	200	300
18 mm				9.6 g	16.9 g	27.1 g	12.3 g	22.1 g	37.0 g
22 mm				12.3 g	21.6 g	34.5 g	15.0 g	26.8 g	44.4 g
25 mm				15.3 g	27.5 g	43.1 g	18.0 g	32.7 g	53.0 g
28 mm	2.7 g	5.2 g	9.9 g	15.9 g	29.9 g	45.5 g	18.6 g	35.1 g	55.4 g
32 mm				20.2 g	39.0 g	59.0 g	22.9 g	44.2 g	68.9 g
35 mm				21.1 g	39.5 g	59.5 g	23.8 g	44.7 g	69.4 g
38 mm				24.9 g	46.9 g	69.9 g	27.6 g	52.1 g	79.8 g



	Ass	Assembly Process using IT5HM and IT5D Receptacles							
	Receptacle (IT5HM) after cap / tape is removed			after	ecepta (IT5HM Interpo nstalle	l) oser is	two (IT5I	rposer Recept HM & fter fir ssemb	tacles IT5D) nal
Stacking				Cont	act pos	sition			
Height	100	200	300	100	200	300	100	200	300
19 mm				10.4 g	18.4 g	30.0 g	13.1 g	23.6 g	39.9 g
23 mm				13.1 g	23.1 g	37.4 g	15.8 g	28.3 g	47.3 g
26 mm				16.1 g	29.0 g	46.0 g	18.8 g	34.2 g	55.9 g
29 mm	3.5 g	6.7 g	12.8 g	16.7 g	31.4 g	48.4 g	19.4 g	36.6 g	58.3 g
33 mm				21.0 g	40.5 g	61.9 g	23.7 g	45.7 g	71.8 g
36 mm				21.9 g	41.0 g	62.4 g	24.6 g	46.2 g	72.3 g
39 mm				25.7 g	48.4 g	72.8 g	28.4 g	53.6 g	82.7 g



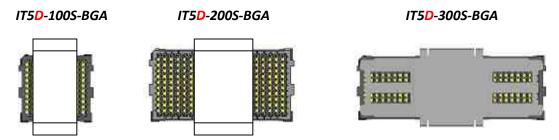
	Ass	sembly	Proce	Assembly Process using IT5M and IT5HD Receptacles							
	Recept after of		ape is	after	otacle (Interpo Installe	oser is	two (IT5I a	rposer Recept M & IT fter fir ssemb	tacles 5HD) aal		
Stacking				Cont	act po	sition					
Height	100	200	300	100	200	300	100	200	300		
19 mm				9.6 g	16.9 g	27.1 g	13.1 g	23.6 g	39.9 g		
23 mm				12.3 g	21.6 g	34.5 g	15.8 g	28.3 g	47.3 g		
26 mm				15.3 g	27.5 g	43.1 g	18.8 g	34.2 g	55.9 g		
29 mm	2.7 g	5.2 g	9.9 g	15.9 g	29.9 g	45.5 g	19.4 g	36.6 g	58.3 g		
33 mm				20.2 g	39.0 g	59.0 g	23.7 g	45.7 g	71.8 g		
36 mm				21.1 g	39.5 g	59.5 g	24.6 g	46.2 g	72.3 g		
39 mm				24.9 g	46.9 g	69.9 g	28.4 g	53.6 g	82.7 g		



	Asse	embly	Proces	s using	IT5HN	1 and IT	5HD Re	ecepta	cles
	(ITS	ceptac SHM/H cap / ta emove	ID) ape is	after	ecepta (IT5HM Interpo nstalle	l) oser is	two (IT5H a	rposer Recept IM & I ⁻ fter fir ssemb	tacles ISHD) aal
Stacking				Cont	act po	sition			
Height	100	200	300	100	200	300	100	200	300
20 mm				10.4 g	18.4 g	30.0 g	13.9 g	25.1 g	42.8 g
24 mm				13.1 g	23.1 g	37.4 g	16.6 g	29.8 g	50.2 g
27 mm				16.1 g	29.0 g	46.0 g	19.6 g	35.7 g	58.8 g
30 mm	3.5 g	6.7 g	12.8 g	16.7 g	31.4 g	48.4 g	20.2 g	38.1 g	61.2 g
34 mm				21.0 g	40.5 g	61.9 g	24.5 g	47.2 g	74.7 g
37 mm				21.9 g	41.0 g	62.4 g	25.4 g	47.7 g	75.2 g
40 mm				25.7 g	48.4 g	72.8 g	29.2 g	55.1 g	85.6 g

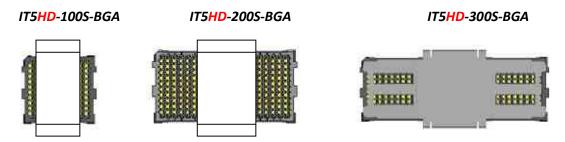


2.2.2 IT5 Detachable Receptacle with cap or tape



Contact Positions	Part Number	Weight
100 (100 signals/110 grounds)	IT5D-100S-BGA(**)	2.7 g
200 (200 signals/220 grounds)	IT5D-200S-BGA(**)	5.2 g
300 (300 signals/330 grounds)	IT5D-300S-BGA(**)	9.9 g

^{*} Receptacle choice will achieve more variety of stacking heights

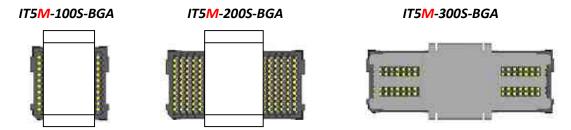


Contact Positions	Part Number	Weight
100 (100 signals/110 grounds)	IT5HD-100S-BGA(**)	3.5 g
200 (200 signals/220 grounds)	IT5HD-200S-BGA(**)	6.7 g
300 (300 signals/330 grounds)	IT5HD-300S-BGA(**)	12.8 g

^{*} Receptacle choice will achieve more variety of stacking heights

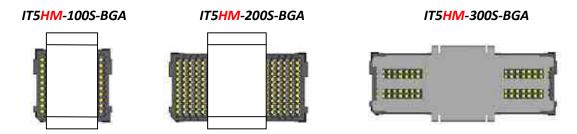


2.2.3 IT5 Mounting Receptacle with cap or tape



Contact Positions	Part Number	Weight
100 (100 signals/110 grounds)	IT5M-100S-BGA(**)	2.7 g
200 (200 signals/220 grounds)	IT5M-200S-BGA(**)	5.2 g
300 (300 signals/330 grounds)	IT5M-300S-BGA(**)	9.9 g

^{*} Receptacle choice will achieve more variety of stacking heights

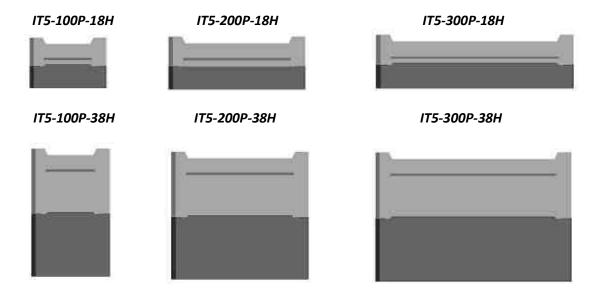


Contact Positions	Part Number	Weight
100 (100 signals/110 grounds)	IT5HM-100S-BGA(**)	3.5 g
200 (200 signals/220 grounds)	IT5HM-200S-BGA(**)	6.7 g
300 (300 signals/330 grounds)	IT5HM-300S-BGA(**)	12.8 g

^{*} Receptacle choice will achieve more variety of stacking heights



2.2.4 Interposer



IT5 Interposer Height Variation

Stacking	Contact Position									
Height	100		200		300					
110.5	Part Number	Weight	Part Number	Weight	Part Number	Weight				
18 mm	IT5-100P-18H	6.9 g	IT5-200P-18H	11.7 g	IT5-300P-18H	17.2 g				
22 mm	IT5-100P-22H	9.6 g	IT5-200P-22H	16.4 g	IT5-300P-22H	24.6 g				
25 mm	IT5-100P-25H	12.6 g	IT5-200P-25H	22.3 g	IT5-300P-25H	33.2 g				
28 mm	IT5-100P-28H	13.2 g	IT5-200P-28H	24.7 g	IT5-300P-28H	35.6 g				
32 mm	IT5-100P-32H	17.5 g	IT5-200P-32H	33.8 g	IT5-300P-32H	49.1 g				
35 mm	IT5-100P-35H	18.4 g	IT5-200P-35H	34.3 g	IT5-300P-35H	49.6 g				
38 mm	IT5-100P-38H	22.2 g	IT5-200P-38H	41.7 g	IT5-300P-38H	60.0 g				

Please note that a uniquely keyed interposer cannot be used with general receptacles.



2.3 Part Number / Manufacturing Lot Number

2.3.1 Part Number Designation

Receptacle

Interposer

IT5xxx - xxx S - BGA xx (xx)IT5xx - xxx P - xxH xx (xx)(1)(2)(3)(4)(5) (6) (7) (1)(8) (3) (4) (9) (6) (10)

Plug

IT5Mx - xxx P - xxBGA xx (xx)

(1)(2) (3) (4) (9) (5) (6) (7)

Series name

No Further Designation

Receptacle Type

IT5D-xxxS-BGA: Detachable (Mating) Receptacle

IT5Dx-xxxS-BGA: Detachable (Mating) Receptacle (Customized)

IT5HD-xxxS-BGA: +1mm Detachable (Mating) Receptacle

IT5HDx-xxxS-BGA: +1mm Detachable (Mating) Receptacle (Customized)

IT5M-xxxS-BGA: Mounting Receptacle

IT5Mx-xxxS-BGA: Mounting Receptacle (Customized)

IT5HM-xxxS-BGA: +1mm Mounting Receptacle

IT5HMx-xxxS-BGA: +1mm Mounting Receptacle (Customized)

IT5M-xxxP-xxBGA: Plug

IT5Mx-xxxP-xxBGA: Plug (customized)

Contact Positions

100, 200, 300

Connector

S: Socket P: Plug

BGA: Ball Grid Array

No Further Designation

Package Specification

Blank: Standard xx: Customized

Material and Plating Specification of Receptacle

(37): Pb-free Solder: Sn (96.5) Ag (3.0) Cu (0.5) Contact Area: Gold(0.76 µm)+Ni(1.5 µm) (M-side receptacle only) housing color: black



(39): Pb-free Solder: Sn (96.5) Ag (3.0) Cu (0.5)

Contact area: Gold(0.76 μ m)+Ni(1.5 μ m) (D-side receptacle only) housing color: gray

(8) Interposer Type

Blank: Standard xx: Customized

(9) Interposer Wafer Height (mm)

18, 22, 25, 28, 32, 35, 38

(10) Plating Specification of Interposer

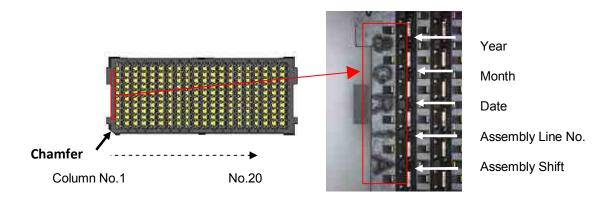
(03): Contact Area: Gold(0.76 μm)+Ni(1.5 μm)



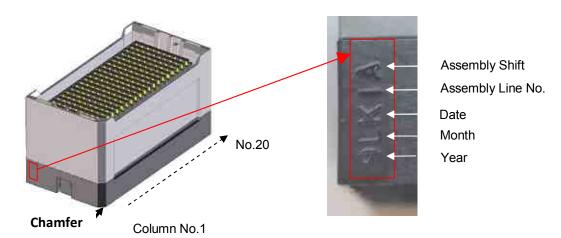


2.3.2 Manufacturing Lot Number

Receptacle (Ex. 200pos)



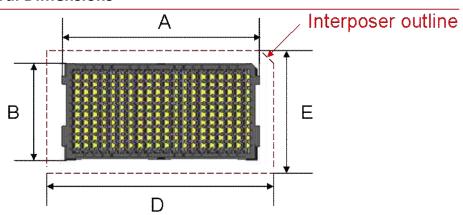
Interposer (Ex. 200pos)





^{*} Lot number indication may subject to change.

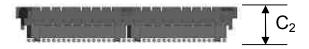
2.4 Receptacle General Dimensions



Dimension A, B, D, and E are the same for regular receptacle and +1 receptacle



Shown: 200 position mounting receptacle, IT5M-200P-BGA



Shown: 200 position +1 mounting receptacle, IT5HM-200P-BGA

		Contact Position		
		100	200	300
No. of Signal Contacts		100	200	300
No. of Ground Contacts		110	220	330
Α	Receptacle Length	21	38.5	56
В	Receptacle Width	19.2	19.2	19.2
C ₁	Regular Receptacle Height	6	6	6
C ₂	+1 Receptacle Height	7	7	7
D	Interposer/Plug Outline Length	24	41.5	59
E	Interposer/Plug Outline Width	21	21	21

*All dimensions shown are in mm



Section 3 Operating Characteristics

This section of the Design Note discusses material, electrical, mechanical, and environmental characteristics. It also discusses BGA reliability testing.

3.1 Material

Numbering of component is same as customer drawing.

3.1.1 Receptacle

NO	Component	Material	Finish & Remarks	
1	Housing	LCP	Black or Gray, UL 94V-0	
2	Locator	LCP	Black , UL 94V-0	
3	Contact	Copper Alloy	Contact Area : Gold (0.76 micron) over Nickel (1.5 micron) Mounting Area : Gold (0.03 micron) over Nickel (1.5 micron) Other : Nickel (1.5 micron)	
4	Solder Ball	Tin (Pb-Free)	Sn(96.5)-Ag(3)-Cu(0.5)	
5	Tray	Polystyrene	Gray	
6	Pick Up Cap	Stainless steel	300pos	
	Pick Up Tape	Paper(Nomex)	100pos and 200pos	

3.1.2 Interposer

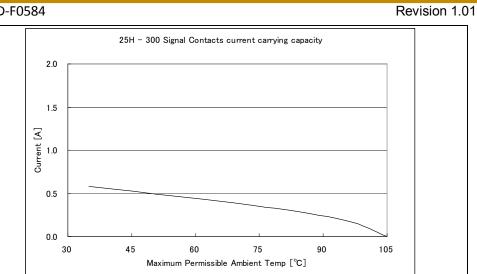
NO	Component	Material	Finish & Remarks
1	Guide(Mounting Side)	PBT	Black , UL 94V-0
2 Guide(Detachable Side)		LCP	Gray , UL 94V-0
		PBT	Gray , UL 94V-0
3	Blade	LCP	Black , UL 94V-0
4	Contact	Copper Alloy	Contact Area : Gold (0.76 micron)
_	• 101111	,	over Nickel (1.5 micron)
5	Ground Shield	Copper Alloy	Other : Nickel (1.5 micron)
6	Tray	Polypropylene	_



3.2 Electrical

Test	Test Condition	Requirement	Typical Value
Low Level Contact Resistance* (LLCR)	EIA-364-23	60 mΩ MAX $(18 - 20$ H) 70 mΩ MAX $(21 - 24$ H) 80 mΩ MAX $(25 - 28$ H) 90 mΩ MAX $(29 - 32$ H) 100 mΩ MAX $(33 - 36$ H) 110 mΩ MAX $(37 - 40$ H) $(H: stacking height in mm)$	
Insulation Resistance (IR)	EIA-364-21	1000M ohm MIN	Over 20,000M ohm
Dielectric Withstanding Voltage (DWV)	EIA-364-20 AC 150V for 60 seconds Different contacts than LLCR	No disruptive discharge No leakage current : 2mA MAX	Break voltage: over 800V
Current Rating	25H - 30 110 100 90 80 0 70 100 90 80 0 0 0 0 0 0 0 0 0 0 0	00 Signal Contacts Temperatures v	
	10 Ambient Temp 0 0.0 0.2		0.6 0.8





^{*} The value of contact resistance includes 2 contact points and the bulk resistance



3.3 Mechanical

3.3 Mechanical Test	Test Condition	Requirement	Typical Value
Mating / Unmating Force	EIA-364-13	Mating: 45 N MAX (100pos) 90 N MAX (200pos) 135 N MAX (300pos) Unmating: 5N MIN (100pos) 10N MIN (200pos) 15N MIN (300pos)	Mating: 40 N (100pos) 80 N (200pos) 120 N (300pos) Unmating: 20N (100pos) 35N (200pos) 55N (300pos)
Durability	EIA-364-09 Cycle rate: 300 maximum per hour 100 times (detachable side) 5 times (mounting side)	No evidence of physical damage	-
Random Vibration	EIA-364-28, Condition V, letter D 90 min in each 3 directions Electrical lord condition : 100mA max	Less than 1micro second	-
Sinusoidal Vibration	GR1217 Section 9.1.2.1 EIA-364-28B, condition II 10-500Hz in each 3 directions 2H 10G	Less than 1micro second	-
Mechanical Shock	GR1217 Section 9.1.2.1 EIA-364-27, condition I 3 directions each, 50G, 11ms, 18 times	Less than 1micro second	-
Packing	ISTA-3A	No evidence of physical damage BGA co-planarity: 0.18mm max	-
Contact Normal Force	- 0.3N min 1.2 1.1 1 0.9 0.8 0.7 2.06 0.5 0.4 0.3 0.2 Minim		num Gap num Gap au LG
Contact Wiping Length	1.4+/-0.3 mm (without recommended spacers) 1.0+/-0.3 mm (with recommended spacers) Refer to page 42 for recommended spacer information		
Contact Retention Force	1.5N min / signal contact -		-
BGA Co-planarity	0.18 mm Max		-



3.3.1 Cross Section

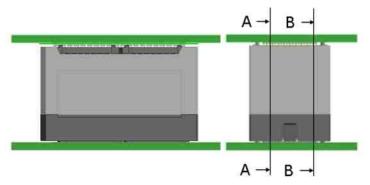
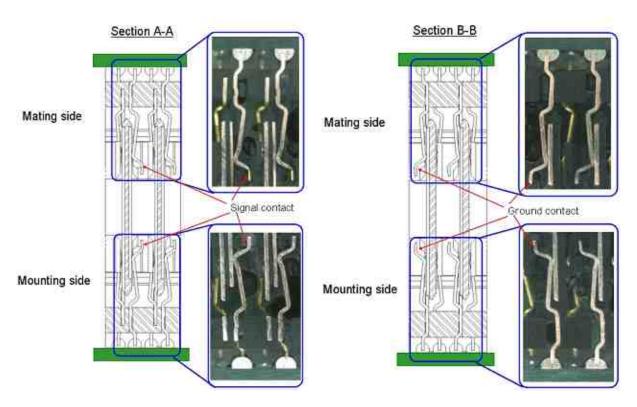


Figure 3-1

Signal contact

Ground contact





3.4 Environmental

We guarantee 10 years of storage per satisfactory results from accelerated high temperature tests that store connectors at 105 °C for more than 120 hours according to EIA-364-1000.01. The specification has Table 8 - Test durations (hours) for temperature life which indicates the previously-mentioned accelerated test condition equal to 60 °C (typical maximum temperature for office environment set by one of our major customers) for 10 years.

The performance of our connectors is satisfactory within an environmentally-related corrosive atmosphere according to EIA-364-65. Test procedure that covers this specification allows the observation of how plated and unplated surfaces react when exposed to different concentrations of flowing gas mixtures.

Test	Test Condition	Requirement	Remarks
Thermal Shock	EIA-364-32 Condition 1 -55 to 85 °C, 10cycles Recovery : 1/2 hour minimum	No evidence of physical damage Resistance change: 20 milliohms MAX	-
Cyclic Temperature & Humidity	EIA-364-31, EIA-364-1000.01, Table 2 Conditioning : dry oven at 50 °C, 24h Rest condition : see Appendix 2 Recovery : 5 h	No evidence of physical damage Resistance change: 20 milliohms MAX	-
Humidity	EIA-364-31 condition A 500h , 90-95% , 42 +/-2 °C	No evidence of physical damage Resistance change: 20 milliohms MAX	-
Temperature Life	EIA-364-17, Method A, condition 3 85 °C, 500h	No evidence of physical damage Resistance change: 20 milliohms MAX	-
Cold	IEC-60512-11-10 (JIS C 5402 7.9) -55 °C, 96h	No evidence of physical damage Resistance change: 20 milliohms MAX	-
Salt Spray	IEC-60512-11-6 (JIS C 5402 7.1) Salt 5 wt% , 35 °C, 48h	No evidence of physical damage Resistance change: 20 milliohms MAX	-
Mixed Flowing Gas	EIA-364-65, Class IIA Concentration (ppb) Cl2: 10±3 NO2: 200±50 H2S: 10±5 SO2: 100±20 RH%: 70±2 Temp °C: 30±1 Exposure: 14days (Unmated 7days, mated 7days) Recovery: 2hrs minimum	No defect such as corrosion which impairs the function of connector Resistance change: 20 milli- ohms MAX	-



3.5 BGA Reliability

These tests apply to lead free applications.

Test	Test Condition	Requirement	Remarks
Thermal Shock	IPC-9701 6000 cycles between 0 and 100 °C	No more than 20% increase from the initial resistance while monitored for five consecutive reading scans	-
Solder Ball Shearing	IPC-9701, 6000 cycles between 0 and 100 °C Shearing speed is 500 mm / second	No inter metallic failure between contacts and balls	-
High Temperature Storage	Refer to IPC-9701, 105 °C, 1000 hours	No more than 20% increase from the initial resistance while monitored for five consecutive reading scans	-
	IPC-9701 6000 cycles between 0 and 100 °C	SnCu inter-metallic layers observed at 'Solder to Connector Pin' interface, and at 'Solder to Pad' interface	-
Cross Section	X-Ray Image Cross Section Target	Typical Solder Joints	after Thermal Shock
	Solder to Pad 10 micron	Solder to 10 micron	Connector Pin



Section 4 Signal Integrity

This section of the Design Note illustrates the overview, 25Gbps solution, differential performance and propagation delay on Hirose's IT5 signal integrity performance.

4.1 Overview

By meeting the stringent (extrapolated) insertion-loss-to-crosstalk-ratio (ICR) specifications as defined in the IEEE802.3ap standard, IT5 is fully capable of supporting 10, 20 or 25+ Gbps differential data transmission.

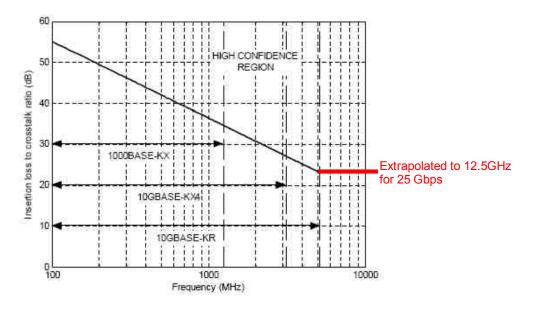


Figure 4-1

For high-speed data transmission, the transmitters (TX) and receivers (RX) are usually grouped separately, in order to minimize the effect of near-end crosstalk (NEXT). Actual measurements were taken on 120mil test boards (Figure 4-2) with IT5-35mm insert molding connector, 2 via transitions through mid routing layers, and 6"+6" FR408 PCB traces.



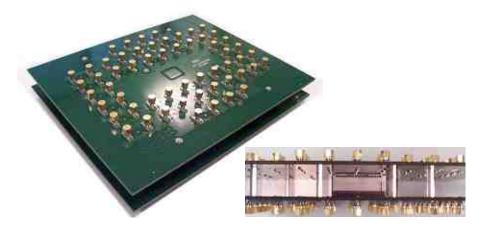


Figure 4-2 Demo board

The following ICR curve (Figure 4-3) corresponds to the power sum of far-end crosstalk (FEXT) from 8 aggressor pairs and 1 victim pair in 3 connector columns. It is clear that IT5 meets the ICR spec. for 25 Gbps data rate in this configuration (Figure 4-4).

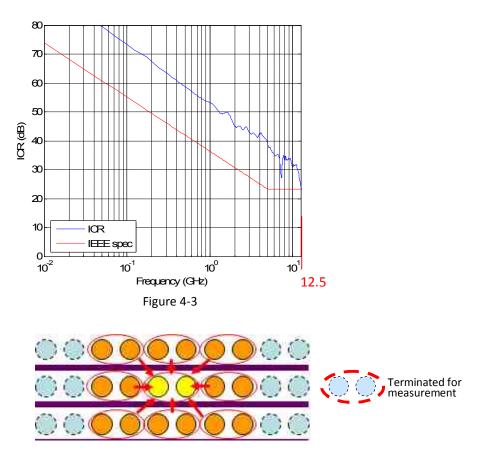


Figure 4-4 FEXT pin configuration



Document Number: ETAD-F0584 **4.2 Differential Signals**

To examine the behavior of the IT5 connector by itself, 62mil characterization boards (see Figure 4-5) were measured with their 1.6" lead-in traces de-embedded. Center pair, 8, will always be used as a cross talk victim throughout this section. (See Figure 4-6)

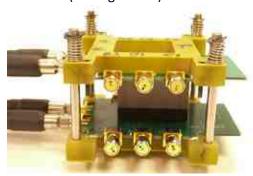


Figure 4-5 Characterization board

Figures 4-7 to 4-10 show the measured vs. simulated differential insertion loss (IL), return loss (RL), nearend crosstalk (NEXT), and far-end crosstalk (FEXT) between two nearest neighbors in an IT5-35mm connector (Figure 4-6). Data at other stack heights are detailed in Section 4.4.

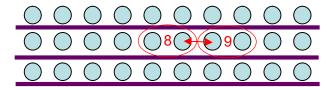


Figure 4-6 Illustration of the victim and nearest neighbor pairs

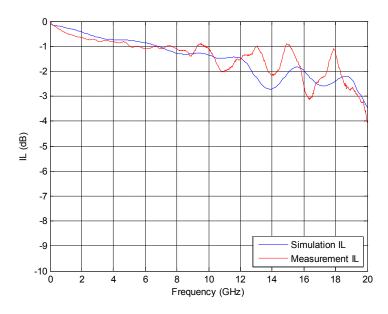


Figure 4-7 Differential insertion loss



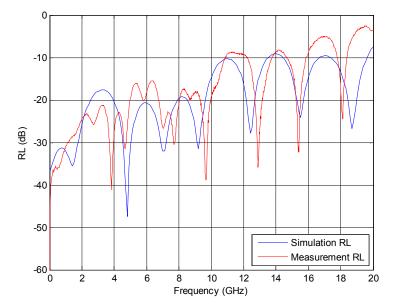


Figure 4-8 Differential return loss

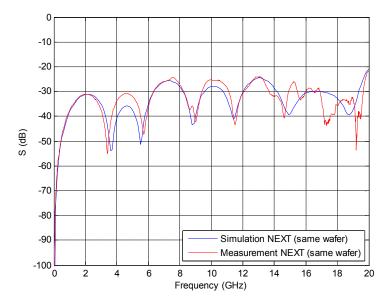


Figure 4-9 Differential NEXT



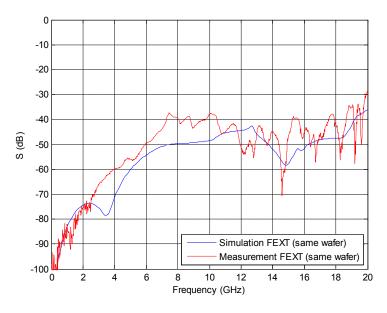


Figure 4-10 Differential FEXT

Figures 4-12 and 4-13 show the simulated NEXT and FEXT among various differential pairs of an IT5-35mm connector in a fully-populated configuration (Figure 4-11). Near-end pair index is shown in Figure 4-11. For far-end pair assignments, 15 is added to corresponding near-end aggressor index. For example, same-wafer nearest neighbor, which is differential pairs 8 and 7 in near-end, will be 8 and 22 for FEXT index. (see Figure 4-13). Only crosstalk data from aggressors 1, 2, 3, 6 and 7, and corresponding far end sources, are plotted since the remaining aggressors are symmetric pairs and will be duplicate graphs for simulation.

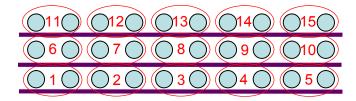


Figure 4-11 Near-end port assignments



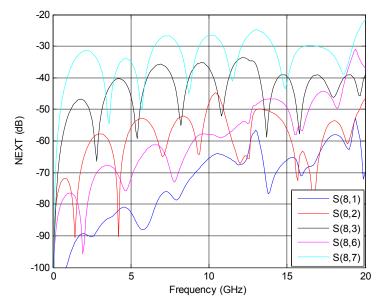


Figure 4-12 Differential NEXT

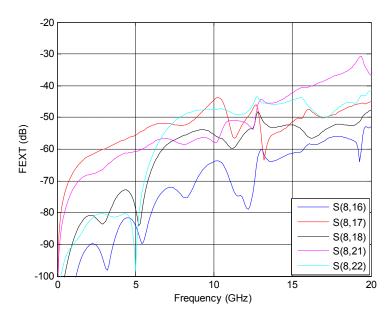


Figure 4-13 Differential FEXT



Figure 4-14 shows the impedance profile of IT5-35mm connector at 30ps, 50ps and 100ps (20% to 80%) rise time. Note that IT5's sockets have slightly higher impedance by design, in order to compensate the generally low-impedance transition from connector to PCB traces through vias.

IT5 Receptacle region

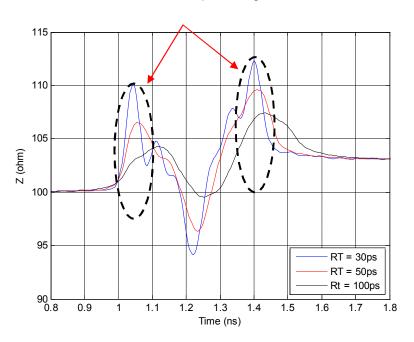


Figure 4-14 Differential impedance



4.3 Differential S Parameters of 25 and 35 mm Height

Figures 4-16 to 4-17 show the measured differential return loss, insertion loss, NEXT, and FEXT for IT5 of 25mm and 35mm stack heights.

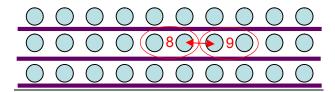


Figure 4-15 (NEXT and FEXT)

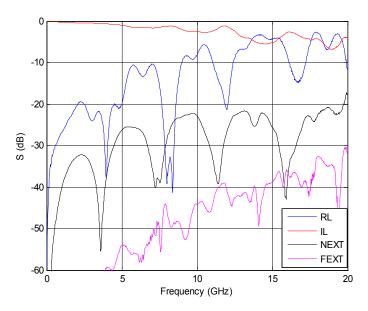


Figure 4-16 Measured differential response for IT5-25mm



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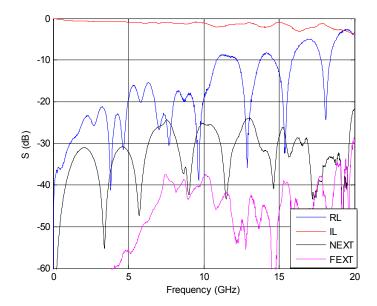


Figure 4-17 Measured differential response for IT5-35mm

4.4 Propagation Delay

The following table shows simulated propagation delays through IT5 connectors with stack heights of 18, 28 and 35mm at 1 GHz.

Stack Height (mm)	Propagation Delay (ps)
(11111)	Differential
18	116.21
28	173.14
35	201.07

Table 4-1 Propagation delay



Section 5 PWB Design

The Hirose IT5 connector's footprint is a staggered area array that allows space for easy via placement and signal routing between pads. Each row of I/O's alternates signal and ground interconnections. It is mounted to the board as a lightweight receptacle, and an interposer is used to connect to parallel PWBs at multiple different height options. Spacers must be used in conjunction with the interposers to help reinforce the structure of the final multi-PWB assembly.

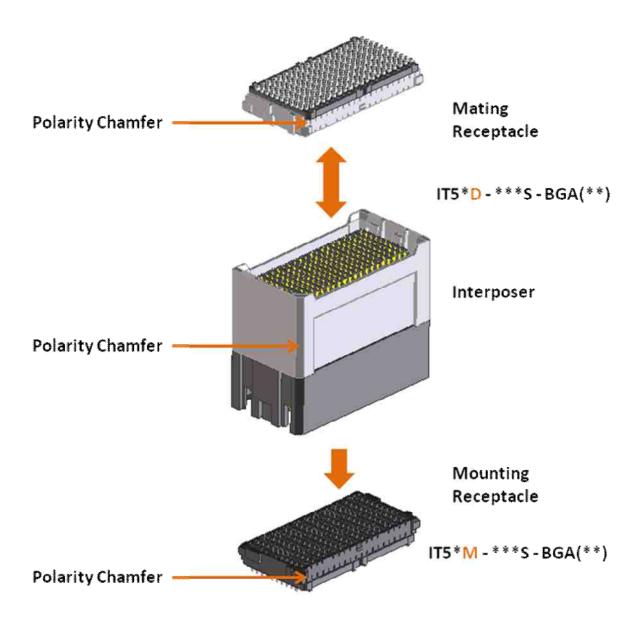
This section of the Design Note discusses multi-connector systems, clearance between connectors, interposer direction, and alignment tolerances.



Document Number: ETAD-F0584 **5.1 Component Footprint**

5.1.1 Polarity

Each receptacle and interposer has **one corner chamfered** to insure proper orientation during assembly and installation. The corner with the **chamfer is nearest to pin A1**.



Shown: IT5-200-35H

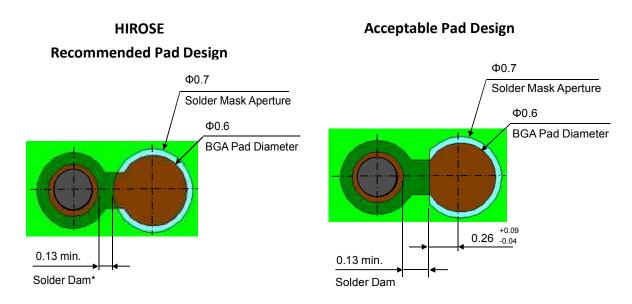


Annotation

For **visual inspection** purposes, **"Pin 1"** should be denoted on the silkscreen of the PWB by a **specific marking** (e.g. asterisk or other accepted symbol) near the A1 contact location and chamfer.

5.1.2 Pad Specification

0.6mm diameter Non-Solder Mask Defined (NSMD), also known as *copper defined* or *metal defined*, pads are recommended. Recommended sizes and clearances are shown below:

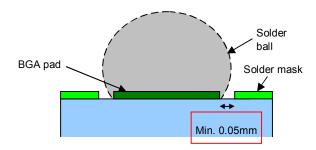


* All dimensions shown are in mm

Remarks

For other via design, such as Via in Pad, design examples are described in the IT5 PCB design application note (13HSI-S017) .





Cross Section of Pad and Solder ball

Keep minimum clearance 0.05mm between BGA pad and solder mask to achieve "copper defined BGA pad".

BGA pad finish: OSP (Organic Solderability Preservative) or HASL (Hot Air Solder Leveler).

The drill diameter of 0.34mm is for reference only. Use the proper aspect ratio of board thickness to via drill diameter for each PCB fabricator.

Through-via sizes will depend on PWB thickness and fabricator's capabilities. Vias should be placed far enough from the pad to ensure a minimum solder dam width of 0.13mm. Circular openings in the solder mask are preferred, but D-shape openings are acceptable if the minimum spacing requirement is met.

PWB pad finish is typically **Organic Solderability Preservative (OSP)** or **Hot Air Solder Level (HASL)**, but the component can also be used with Electroless Nickel-Immersion Gold (ENIG), Immersion Silver and Immersion Tin.

The **stencil apertures** should be **0.54mm circles**, concentric with the copper pads. This represents a 10% reduction from the diameter of the pad to compensate for typical variations in the assembly process.

The specified clearance, or **solder mask relief**, from the copper feature **is 0.05mm**.

<u>Precaution</u>

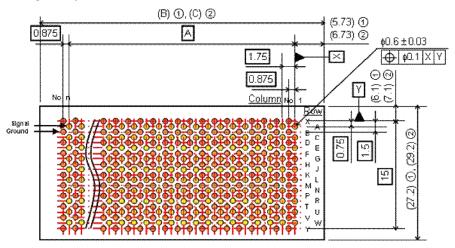
Verify fabricator capability. Solder mask registration must be accurate to at least **0.05mm**. PWB fabricator's registration capability should be verified. Depending on the thickness of PWB, fabricator's **aspect ratio** capabilities **for through vias** should also be verified.





5.1.3 Component Footprint and Contact Assignment

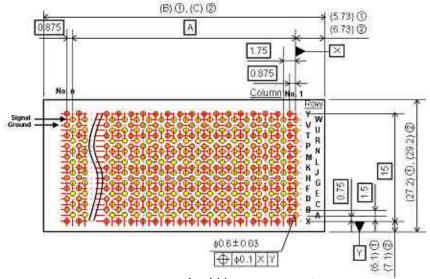
Mounting Receptacle - IT5*M



IT5*M-***S-BGA Footprint

Detachable Receptacle - IT5*D

① Minimum clearance for all devices



IT5*D-***S-BGA Footprint

Signal PadGround Pad

Minimum clearance for sensitive devices Ground Pad			
Dimension (mm)	100	200	300
A	15.75	33.25	50.75
В	28.10	45.60	63.10
С	30.10	47.60	65.10

^{*} All dimensions shown are in mm.



5.1.4 Pin Connections

Figure 1 shows an example of standard pin connections of a mounting side (IT5M receptacle) and a detachable side (IT5D receptacle). For the best use of IT5 FEXT cancellation technology, twisted pairs and non-twisted pairs are placed alternately in the same column and staggered between adjacent columns.

Note: IT5-100P-XXH pin connections are shown as an example in Figure 1.

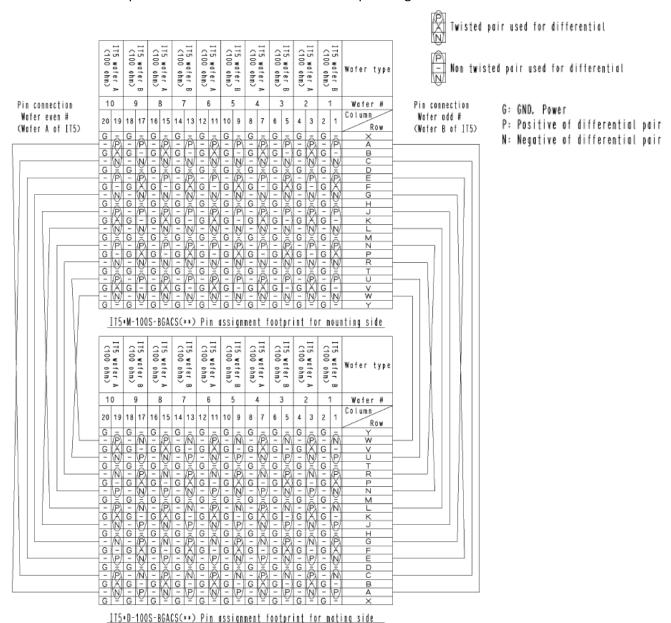


Figure 1 Pin Connections



5.1.5 Contact Assignment

Figure 2 shows the side view of the IT5 connector. Figures 3 and 4 show the pin assignments on the PCB. Odd-numbered columns are signals and the even-numbered columns are grounds.

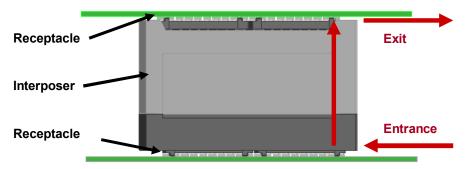
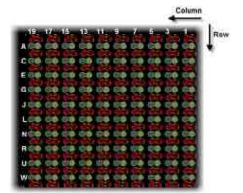
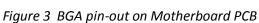


Figure 2 IT5 connector side view





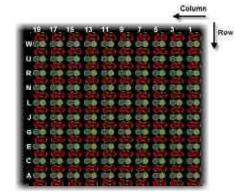


Figure 4 BGA pin-out on Daughterboard PCB



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5.1.6 Routing Suggestions / Examples

The traces are routed in the column direction, avoiding going over the anti-pad. To avoid intra-pair skews, the trace lengths are matched. All trace bends are at 45-degree angles. Routing on adjacent dual strip line layers is not recommended and non-functional signal pads should be removed. Figures 5, 6 and 7 show examples of BGA pad layout, single-ended trace and differential trace routing on the PCB.

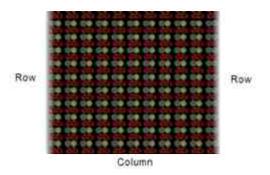


Figure 5 BGA Pad Layout on PCB

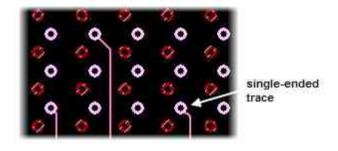


Figure 6 BGA Pad Layout on PCB

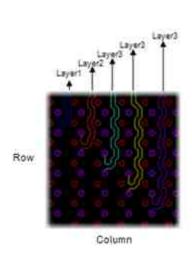


Figure 7-a Differential Routing

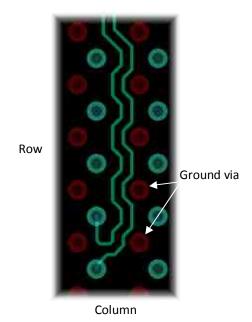


Figure 7-b Details of differential routing design



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As shown in Figure 8, a minimum of three routing layers must be used on the PCB. Also, additional columns and rows of ground vias are added beyond row A, row W, and column 19 (for 100 pos.) to ensure that each signal via on the PCB is surrounded by four ground vias. Figure 9 shows a typical antipad design.

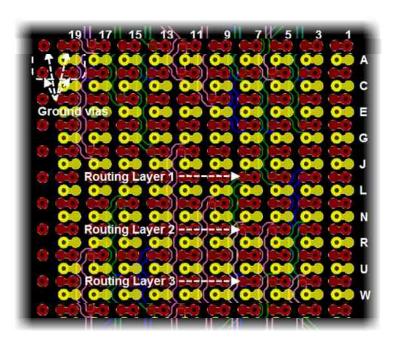
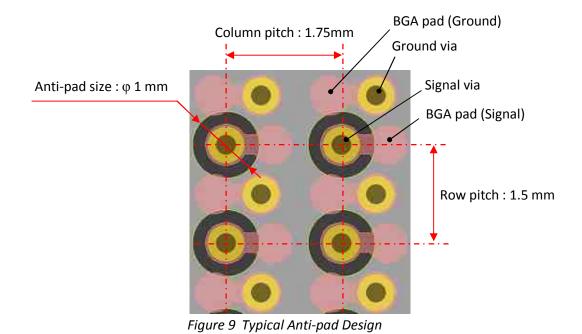


Figure 8 IT5 connector pin-out





A suggested trace routing example for differential signals is shown in Figure 10, with the stack up from Figure 11. The width and spacing of the differential signal traces must satisfy the following criteria:

1. Signal to Signal

$$2*W + S < CP - D - 2*C_{dt}$$

$$2 * W + S < CP - W_a$$

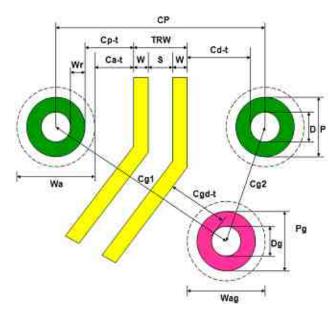
2. Signal to Ground

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$$2*W + S < C_{g1} - \frac{D_g}{2} - C_{gdt} - \frac{D}{2} - C_{dt}$$

$$2*W + S < C_{g1} - \frac{W_a}{2} - \frac{W_{ag}}{2}$$

Single ended traces can be routed anywhere within the limits of the total routing width (TRW) for the differential signals.



NI-	Danamintian.		Refe	rence
No.	Description		Distance	Min. *
1	Column pitch	СР	68.89	
2	Trace	W	3	
3	Spacing	S	5.5	
4	Pad	Р	22	
5	Antipad	Wa	40	
6	Drill	D	12	12
7	Annular Ring	Wr	5	
8	Drill (10:1 ratio)	TRW	16	
9	Clearance Antipad - Trace	Ca_t	5	
10	Clearance Pad - Trace	Cp_t	15	
11	Clearance Drill - Trace	Cd_t	20	20
12	Antipad (for Power)	Wag	30	
13	Pad (GND via)	Pg	22	
14	Drill (GND via)	Dg	12	12
15	Clearance Drill (GND via) - Trace	Cgd_t	10	10
16	Ground via to signal via1	Cg1	56.53	
17	Ground via to signal via2	Cg2	35.43	
•	•	-	-	Limit . maila

Unit : mils

* Minimum dimensions due to process limitations

Figure 10 Trace routing example



Layer No.	Įį.		Mil
		Solder mask	0.5
1	TOP		2.84
		Pre-preg	4.5
2	Ground		0.7
		Core	3
3	Sig 1		0,7
		Pre-preg	3.5
4	Sig 2		0.7
	9.00	Core	3
5	Ground	- 1	0.7
	Ü	Pre-preg	3,5
6	Ground		0.7
		Core	3
7	Sig 3		0.7
		Pre-preg	3.5
8	Sig 4	ii. 2	0.7
	2304510	Core	3
9	Ground		0.7
		Pre-preg	3,5
10	Ground		0.7
		Core	3
11	Sig 5		0.7
	920	Pre-preg	3.5
12	Sig 6	11011-2-3011-3-30	0.7
	Ü	Core	3
13	Ground		0.7
		Pre-preg	3.5
14	Ground	11 2	0.7
		Core	3
15	Sig 7		0.7
	1	Pre-preg	3.5

Layer No.			Mil
16	Sig 8		0.7
	- A	Care	3
17	Ground		0.7
		Pre-preg	3.5
18	Ground		0.7
		Core	3
19	Sig 9		0.7
		Pre-preg	3.5
20	Sig10	11 22	0.7
- ew		Core	3
21	Ground		0.7
		Pre-preg	3.5
22	Ground		0.7
		Core	3
23	Sig11	- Commodel	0.7
	1	Pre-preg	3.5
24	Sig12		0.7
		Core	3
25	Ground		0.7
		Pre-preg	3.5
26	Ground		0.7
		Core	3
27	Sig13		0.7
		Pre-preg	3.5
28	Sig14		0.7
2742	· · · · · · · · · · · · · · · · · · ·	Core	3
29	Ground		0.7
		Pre-preg	4.5
30	воттом		2.84
		Solder mask	0.5
	Total thickr	ess (mil)	121.78

Figure 11 PCB stack up example



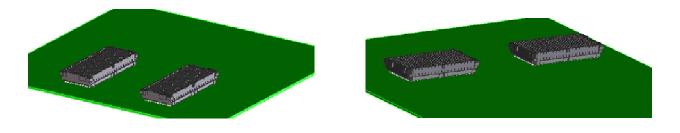
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5.2 Multi-Connector Systems

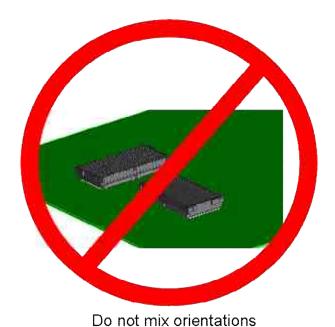
The **IT5** connectors can be used singularly or in combination with other **IT5** connectors.

If multiple connectors are used on the same PWB, they must be oriented in the same direction, as shown below:



Correct Orientations

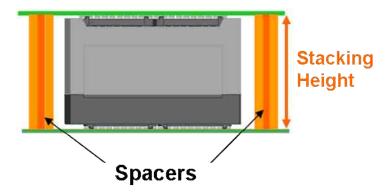
It is not recommended to mix orientations:





5.3 Spacers

Spacers are required to support the PWB's and protect the BGA solder joints.



Suggested spacer style is shown below:

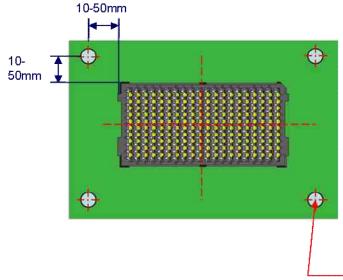


Spacer, male-male, M3 thread

The recommended spacer height corresponds to the example stacking height as shown in the chart below:

Stacking	Recommended
Height	Specer Height
18 mm	18 +/-0.127 mm
22 mm	22 +/-0.127 mm
25 mm	25 +/-0.127 mm
28 mm	28 +/-0.127 mm
32 mm	32 +/-0.127 mm
35 mm	35 +/-0.127 mm
38 mm	38 +/-0.127 mm





Two spacers located diagonally are minimally required. Some applications may require four spacers.

Spacers should be located 10 - 50 mm from the corners of the receptacles to prevent excessive mechanical loading on the interconnections.

If assembly will be subjected to vibration, spacers should be located to prevent resonance, and additional spacers may be required.

Ø 3.5

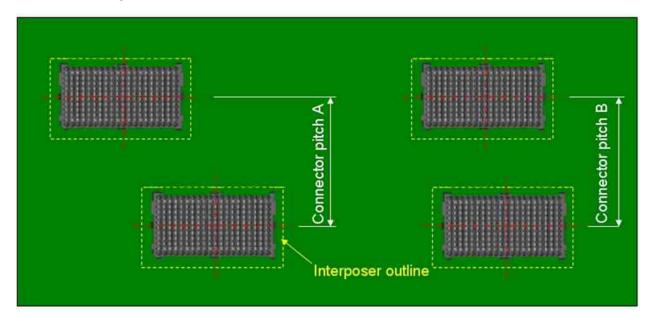
Non plated through hole

Recommended Spacer Location

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5.4 Clearance between Connectors, Other Components, and PCB Edge

Parallel Mounting



Not to scale

(A) If overlap distance is less than half the length of the connector:

Socket Combinations	Connector Pitch A (Min)	Connector Pitch A (Max)
All combinations	24.10 mm	209.20 mm

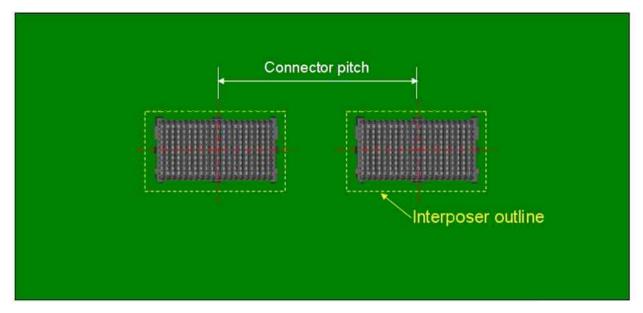
(B) If overlap distance is more than half the length of the connector:

Socket Combinations	Connector Pitch B (Min)	Connector Pitch B (Max)
All combinations	31.00	209.20

Suggested clearances are based on accessibility to grip interposer for purposes of disassembly and field replacement, and verified with multiple mating test boards. For a requirement with a longer connector pitch, please contact a Hirose representative.



Tandem Mounting

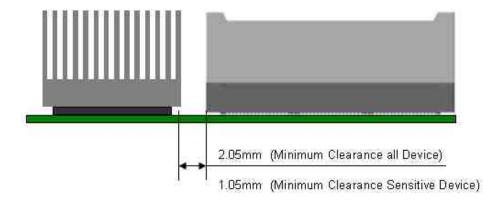


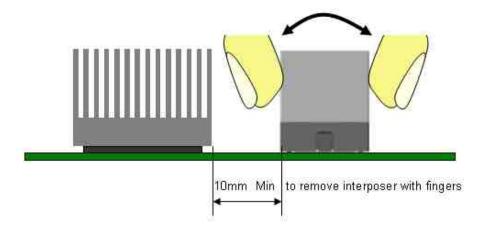
Not to scale

Socket Combinations	Connector Minimum Pitch (mm)	Connector Maximum Pitch (mm)
IT5-100pos + IT5-100pos	26.05	211.00
IT5-100pos + IT5-200 pos	34.80	219.75
IT5-100pos + IT5-300 pos	43.55	228.50
IT5-200pos + IT5-200 pos	43.55	228.50
IT5-200pos + IT5-300 pos	52.30	237.25
IT5-300pos + IT5-300 pos	61.05	246.00



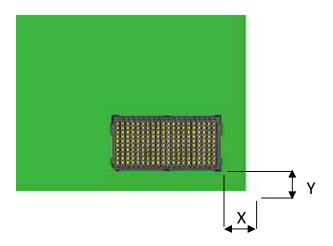
Clearances between a connector and other components





Clearance between the receptacle and PCB edges

Please communicate CEM regarding the clearance especially when requiring the top side reflow.

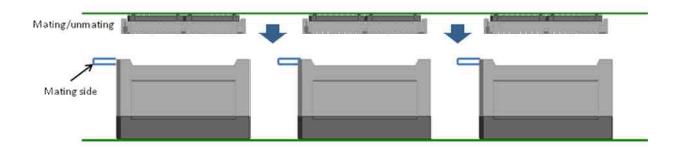




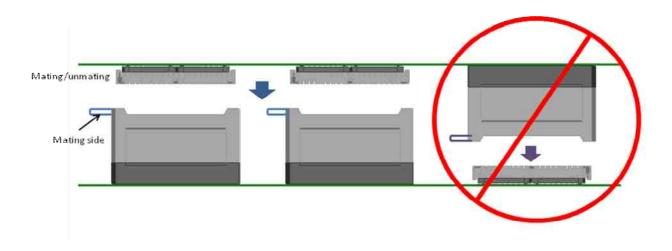
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Do not mix detachable and mounting receptacles on the same PWB.

All interposers must engage in the same direction, as shown below:



Correct Method - all connectors mate in same direction



Incorrect Method – connectors mate in different directions

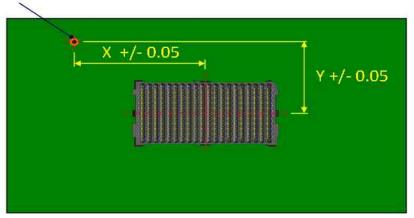


5.6 Alignment Tolerances

5.6.1 Mounting Tolerances

Mounting tolerances of \pm 0.05mm are required for robust SMT assembly and to ensure proper mating fits in cases of multiple connectors:



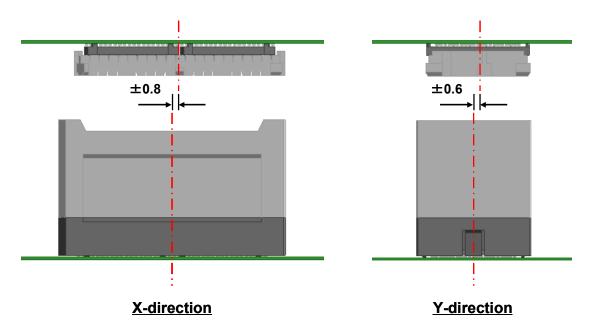


*All dimensions shown are in mm.



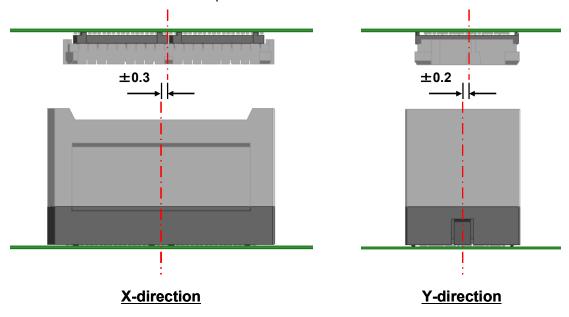
5.6.2 Mating Self Alignment

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5.6.3 Mating Tolerances

Due to its 3-piece design, the IT5 connector system can accept mating tolerances of up to ± 0.3 mm tolerance in the X-axis and up to ± 0.2 mm in the Y-axis.



* All dimensions shown are in mm

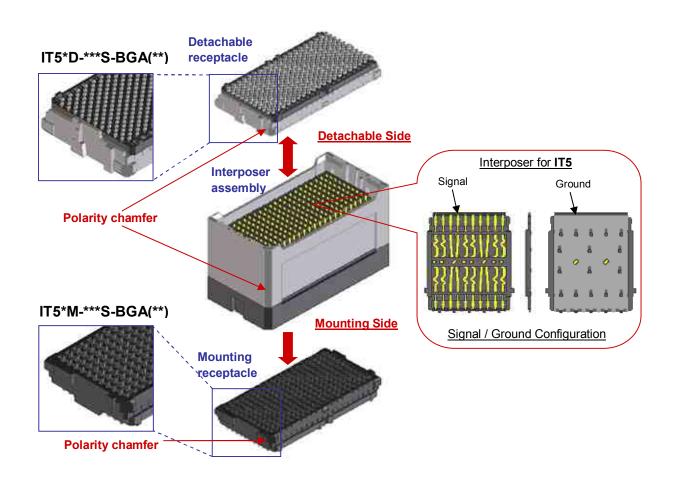


Section 6 Assembly Process

This section of the Design Note discusses summarized IT5 assembly process and interposer installation / removal. As for details, please refer to Assembly note "ETAD-F0458"

6.1 Overall Assembly Process

6.1.1 Difference between Detachable Receptacle and Mounting Receptacle





6.1.2 Assembly Process

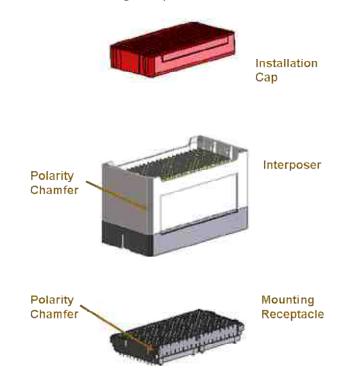
IT5 Assembly Process 1) Reflow Mounting Receptacle (IT5M shown below) on PCB Caution: No Reflow with Interposer 2) Insert Interposer by pressing on Installation Cap, then remove Installation Cap Installation CAP (see page 62) Caution: No touch and push wafers in Interposer 3) Insert Detachable Receptacle (IT5D shown below)



6.2 Interposer Installation

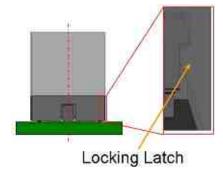
Document Number: ETAD-F0584

The interposer snaps on to the mounting receptacle as shown below:



The snap fit is achieved by a locking latch on each end of the interposer:

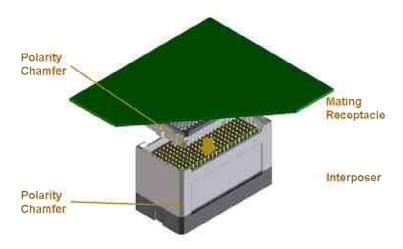
Locking Latch





Revision 1.01

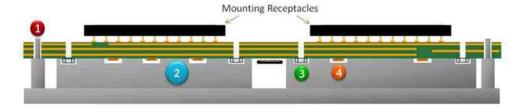
The spacers are installed (not shown) and the detachable receptacle is aligned with the interposer and pressed on as shown below:





It is very important to provide good underside board support when installing the interposers. A simple tooling plate can be fabricated to support the PWB and prevent it from flexing when the interposers are installed:

System Assembly Support Fixture



Key Features of Support Fixture:

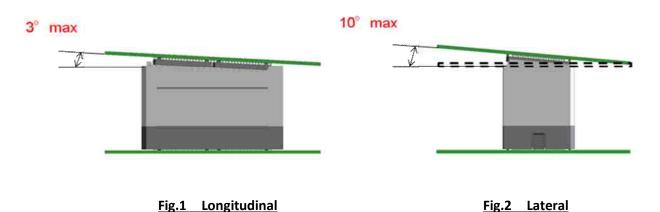
- Guide pins for PWB tooling holes align motherboard to support fixture (shown 2 places)
- Support blocks directly under mounting receptacles prevent board from flexing during interposer and daughter card assembly* (shown 2 places)
- 3 Nests in blocks for spacer nuts hold the nuts in place while the spacer is tightened (shown 4 places)
- Openings in block provide ample clearance for components (shown 5 places)

^{*} For more information on PWB support and allowable deflections, reference IPC-JEDEC 9704, Printed Wiring Board Strain Gage Test Guideline.



The following maximum angles should not be exceeded during manual installation of the daughter card as shown below:

Longitudinal: 3°
 Lateral: 10°

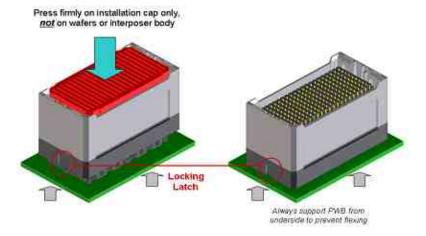


Hirose recommends consideration of the above allowable angles and the orientation of the daughter card for manual assembly during the design process. Hirose also recommends the use of spacers as mentioned on Chapter 5.3 so the tip of the spacers will be fulcrum points that allow operators to accomplish daughter card assembly with small angles.

Position interposer directly over mounting receptacle, aligning the polarity chamfers. If positioned properly, the interposer should slide easily onto the mounting receptacle. Place the installation cap into the interposer, and push the interposer down through the installation cap to engage the locking latches:



Manual Installation

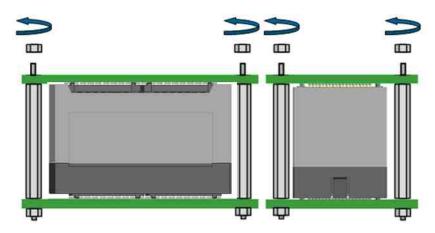


After the interposer is mounted, install spacers onto motherboard (not shown).

6.3 Overall Disassembly Process

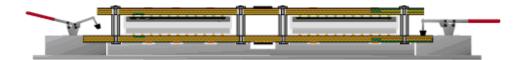
The Hirose **IT5** three-piece connector system can be disassembled if a mother board or daughter card requires replacement. Both the detachable receptacle and the interposer are removable. When removing a card or a connector component, the circuit boards should be handled with great care to prevent damage to them. Failure to properly remove the circuit boards or interposers can result in permanent damage to the circuit assemblies.

To remove a daughter card, first remove the nuts from the reinforcing spacers.

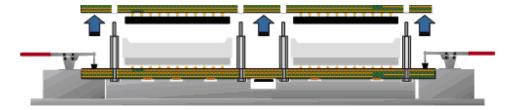


It is very important to prevent excessive flexing of the circuit assemblies during disassembly operations. To minimize flexing of the mother board, a simple tooling plate is suggested.





The tooling plate has clamps to stabilize the mother board while the daughter card (and possibly the interposer) is removed. The daughter card should be lifted straight up off the interposers.



To minimize unnecessary flexing of the daughter card, the removal forces should be applied as close to the interposer as possible without contacting any components. On densely populated assemblies, the edges may be the only open area that can be grasped.

The following maximum angles should not be exceeded during disassembly of the daughter card as shown below:

Longitudinal: 3°

Lateral: 10°

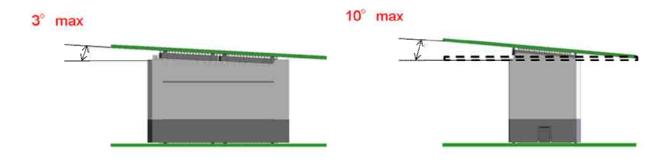


Fig.1 Longitudinal

Fig.2 Lateral

Hirose recommends consideration of the above allowable angles and the orientation of the daughter card for manual disassembly during the design process. Hirose also recommends the use of spacers as mentioned on Chapter 5.3 so the tip of the spacers will be fulcrum points that will allow operators to accomplish daughter card disassembly with small angles.

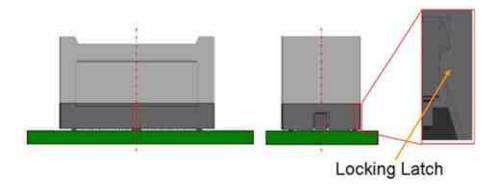


6.4 Interposer removal

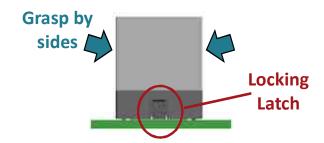
The interposer is secured onto the mounting receptacle with a snap fit tab, as shown below:

The removal shall be 5 times max.

The IT5 interposer is secured onto the mounting receptacle also with other snap fit tabs, shown below.



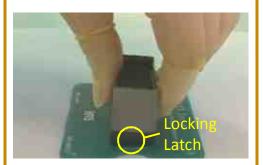
For removal, interposer should be grasped by the sides shown. These sides of the interposer do not have locking latches.



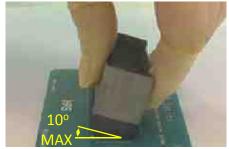


Interposer Removal by Hand

1) Hold the Interposer Assembly on the walls without IT5 locking latches.

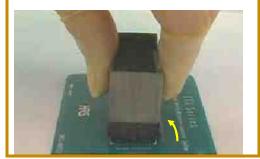


2) Gently rotate one side of the Interposer Assembly laterally 10° maximum

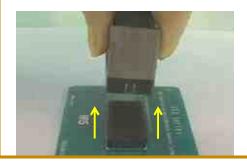


Caution: do not rotate more than 10 degrees

3) While gently rotating, pull up on other side of the Interposer Assembly



4) The Interposer Assembly is removed, and the Mounting Receptacle is ready to accept another Interposer Assembly.

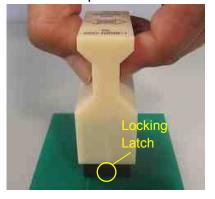




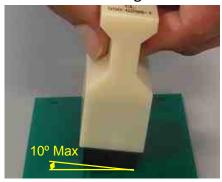
An interposer removal tool is also available*. This tool is not an interposer installation cap, so please do not use it to install an interposer. Doing so may damage an interposer.

Interposer Removal with Tool

1) Cover the Interposer Assembly with the interposer removal tool

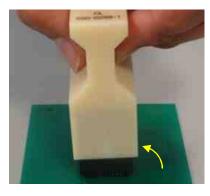


2) Gently rotate one side of the Interposer Assembly laterally 10° maximum using the tool

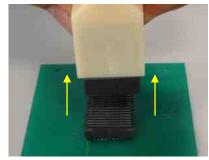


Caution: do not rotate more than 10 degrees

3) While gently rotating, pull up on other side of the tool



4) The Interposer Assembly is removed, as it is inside the tool



Precaution

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Visually inspect the interposer before reinstalling it. Discard if it shows any sign of damage or wear. Do not subject the interposer assembly to more than five removal-reinstallation cycles, even if it appears unaffected.





^{*} See page 62.

6.5 Ordering interposer installation and removal tools

The tables below show CL numbers and product names for interposer installation and removal tools. Please inform Hirose this information when ordering appropriate tool(s).

Installation Tool

Number of Position	CL Number	Product Name
100	CL0636-0900-0-00	IT3-100P-I-CAP
200	CL0636-0901-3-00	IT3-200P-I-CAP
300	CL0636-0902-6-00	IT3-300P-I-CAP

Removal Tool

Number of Position	CL Number	Product Name
200	CL0550-0299-4-00	IT3-200P/REMOVAL-CAP
300	CL0550-0298-1-00	IT3-300P/REMOVAL-CAP



Section 7 Technical Document Library

Following data and documents are available.

7.1 Technical Data

No	Item	Format	File name (Ex.)
1	Simplified 3D model	STEP (SAT &IGES are also available)	IT5M-300S-BGA.stp
2	Footprint data	Allegro	IT5M-300S-BGA.brd
3	Spice models	Spice	IT5-**H.sp
4	Touchstone model	Touchstone	IT5-300-**H.s60p

7.2 Technical Document

No	ltem	Format	File name (Ex.) or Document number
1	2D drawing	PDF	IT5M-300S-BGA.pdf
2	Spec sheets	PDF	IT5M-300S-BGA.pdf
3	Contact reliability report	PDF	TR0636E-10259
4	Lead free thermal cycling test report	PDF	TR0636E-20310
5	Temperature rise report	PDF	TR0636E-20282
6	SI report	PDF	IT5-**H.pdf
7	Assembly note	PDF	ETAD-F0457
8	Design note	PDF	ETAD-F0584
9	Customer demo board test report	PDF	IT5_demo_board_v2.pdf
10	Characterization board test report	PDF	IT5_Characterization_Board_v09. pdf





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